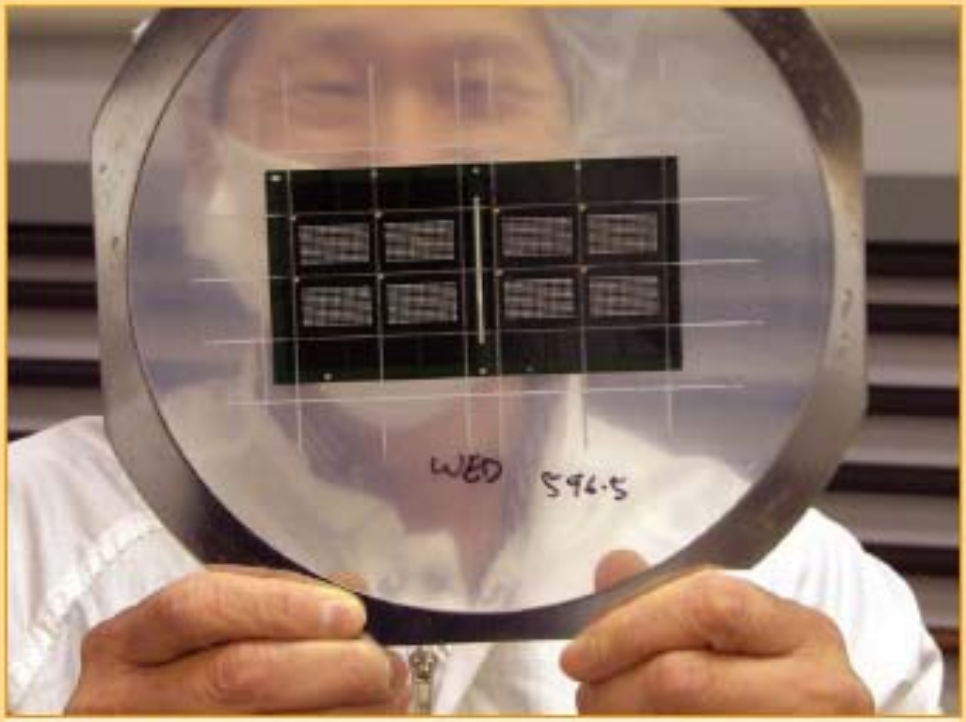
# Singulation: Refining the Kindest Cut of All




Technician holds film frame of BGA devices for tape-based singulation at IPAC, San Jose. *(Chip Scale Review)*

**Separating the die from the wafer, leadframe strip or other carrier through punching or sawing—the two principal methods—is a well-established part of the IC assembly process. The importance of the process, however, is often overlooked due to its rather unglamorous history.**

*By Ron Iscoff, Editor*
*(chipscalereview.com)*

Many IC assembly processes that were once considered simple, operator-intensive chores have taken on a new sophistication with the explosion of chip-scale and wafer-level packaging.

One of these technologies, which can produce a dramatic effect on a company's bottom line, is the separation of the die.

For the sake of brevity, we'll use the term "singulation" to refer to the separation of die from a wafer, other substrate or the cutting of packaged ICs. The tools involved in almost all cases are similar.

At its most elementary, singulation is separating devices from strips or wafers. With leadframe packages, the individual leads are first separated from a leadframe strip.

The dambar that electrically isolates the leads is then removed. Then, the leads are trimmed and formed, and individual packages are separated from the leadframe strip by punch singulation, scribing tools or saws.[1]

## Singulation Methods

Area-array packages, such as ball grid arrays, employ solder balls to form the interconnect path from package to PWB. After reflow, individual packages on laminate strips are singulated by punching, scribing or sawing. The solder balls are inspected for co-planarity, size and position, then placed in trays or on tape and reel.[2]

Dr. Gerald K. "Skip" Fehr, San Jose packaging consultant and industry guru, says future needs in singulation equipment are more of the same: lower cost, higher quality, greater versatility, higher output and better reliability.

For assemblers that use leadframes in smaller volumes, versatile tools that can be programmed to fit different package styles would be beneficial, Dr. Fehr says. "This should be done in conjunction with versatile tools for dedam and form."

## Supplying Small Volume Packages

Dr. Fehr believes this programming would reduce the cost of supplying a small-volume package to customers, since the entry cost of manufacturing the packages would be lower.

CORWIL in Milpitas, Calif., provides singulation during IC assembly.

Banks of saws line the assembly area at NSEB, Bangkok, Thailand.

Another improvement, adds Dr. Fehr, would be on the materials side. "Materials that stay sharper to give longer life and better quality separation would certainly be an improvement. Diamond tools could be a step-up from carbide tools."

Endicott Interconnect Technologies of Endicott, N.Y. [endicottinterconnect.com] focuses on the high-performance chip-carrier market. Products such as the *HyperBGA* chip carrier and the new *CoreEZ* and *HyperZ* carriers present unique challenges at panel singulation, according to John Kresge, senior engineer.

## Advanced Materials

Kresge observes that many advanced materials—copper-clad *Invar* (FeNi36) and complaint PTFE-based dielectrics—do not machine well with conventional mechanical singulation.

*Invar*, which is an iron-nickel alloy, is a "challenging material for producing a clean, uniform edge, as well as preventing loading of the cutting tool with metal particles," Kresge notes.

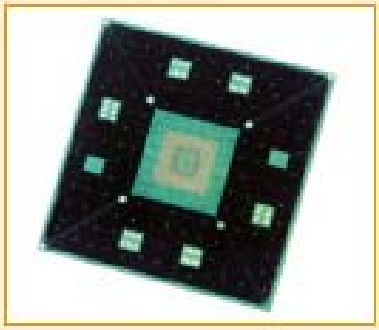
Beyond the need to cut advanced materials cleanly, improved productivity is needed. "The continued rapid growth in the chip-carrier market is driving the desire to increase throughput," Kresge adds.

Kresge also shares a common wish for "smarter" unload systems. "These should be capable of rapid parts unloading and smart sorting, based on the input of known defective pieces.

"Future systems should also be able to sort singulation carriers into carrier trays quickly and discard known defective pieces," Kresge adds. "Time spent unloading carriers is idle time for the cutting process and should be reduced to a minimum."

## Saw Singulation

With CSPs moving into high volume production at increasingly rapid rates, saw singulation is emerging as an efficient



Endicott Interconnect's new CoreEZ chip carrier presents unique challenges at singulation. (EIT)

method of separating densely populated packages, contends Chris Ooi of IPAC, San Jose, [ipac.com] and K.H. Chuah of Greatech [greatech.com.my].

This "proven technology," says Ooi, is directly applicable to BGA, CSP and QFN singulation and offers the flexibility to handle many different package sizes. Saw singulation improves production volume with high throughput, high product quality and lower production costs, Ooi adds.

Automation may take many forms, says Ooi, and demands the flexibility of meeting customer requirements.

Tape-based systems, he says, are "ideal for small-lot production with higher flexibility, but the added tape cost adds significant per-unit expense—especially with large package sizes.

ADT's Series 8000 NextStep Laser Scribing System will accommodate wafers up to 300mm.

Jig-based systems are more cost-effective for high volume production, since there is no need for tape, Ooi reports.

The sawing process, says Ooi, is currently gated by saw feed rates. "Future improvements will be in the form of multi-blade saw heads, improved blade life and six-sided vision inspection."

STATS ChipPAC, Singapore [statschippac.com], one of the largest IC assembly and test houses, produces QFN packages in very large volumes.

## Punch Singulation

The QFN is a popular leadframe-based CSP that can be designed to suit two popular singulation methods, punching and sawing, currently in use at the company.

Punch singulation involves cutting the individual molded IC from a suitably designed leadframe into individual IC packages with equipment that drives a punch and die set.

The punch and die set is usually a dedicated cutting tool designed for a given package dimension and leadcount.

Packages, depending on leadframe configuration, can be singulated into thousands of units an hour, which makes the punch system an attractive choice for

The Disco DFD6340 saw can handle substrate as large as 250 x 210mm.

high-volume applications, explains Jun Bumanlag, senior manager–assembly process engineering, for the company.

Key is the tool's ability to cut the molded units consistently to the required package dimensions. Copper burrs and package chips or cracks on the package edges after punching are important visual mechanical issues that need to be addressed both in the tooling design and equipment, says Bumanlag.

There are a variety of ways to control quality during punch singulation.

The FICO Division of Besi manufactures the *MISS II* for singulation of IC packages and film or metal substrates.

"For the punch and die set, the bottom die tooling must be designed so that it evenly and sufficiently supports the package from the bottom," says Bumanlag.

"These cutting tools employ carbide material that can last up to several thousand cutting cycles or strokes. Development alternatives such as ceramic-based tooling is promising for increased tool life, but could be limited by the difficulty of small tool parts fabrication and cost."

Most of the existing punching tools operate at 50-70 strokes/minute. Higher productivity can be achieved by designing systems with more punching cycles or dual punching stations.

"The vision system must also be suitably enabled for faster and reliable image processing with more units available for inline inspection in a shorter amount of time. The pick-and-place system must also be designed to handle increased throughput requirements," says Bumanlag.

## Wafer Dicing

Dr. Annette Teng Cheung of COWIL Technology [cowil.com], Milpitas, Calif., contends that singulation can easily be the most critical step in semiconductor processing.

"So much torque and force is used during this step that if precautions are not taken, the freed chips may exhibit low strength and chipping damage," she says.

Each wafer exhibits dicing and chipping behavior "unique to that mask-set or design and are particularly influenced by the contents of the dicing lane." The process will become more critical as wafers become more packed, larger, thinner and filled with fragile layers.

Driven by stacked die and miniaturization, the industry has moved towards thinner silicon wafers of less than 100-micron thickness.

"Engineers must establish a delicate balance between conservation of silicon real estate packing up the streets and high-yield singulation," according to Dr. Cheung.

HanMi Semiconductor's integrated, automatic EAD6340K system

Problematic today, she says, is the singulation of highly thinned wafers—without chipping—with high die strength at high throughput rates. "Another challenge is the singulation of brittle wafer materials such as GaAs and SOS wafers, which have a propensity for unacceptable yield-loss levels."

## Dicing Before Grinding

Dicing before grinding (DBG), a commercial process developed by a maker of dicing saws, promises to be a reliable method of singulating highly thinned and fragile dies, says Dr. Cheung.

At ECTC 2006, S. Takyu of Toshiba reported that his group achieved high die strength by combining DBG and chemical-mechanical polishing. Takyu's group demonstrated a 10-micron-thick IC which can be wrapped around the shaft of a straw and pencil.

## Conclusion

Separating the die from its host, whether packaged or unpackaged, is not the labor-intensive task it once was.

Today's saws are not "just saws"—they are elegantly packaged in colorful cabinets and highly automated by software-driven programs. ●

## References


1-2. R. Ulrich and W. Brown, *Advanced Electronic Packaging 2d Edition*, p. 340, Wiley Interscience, 2006.



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