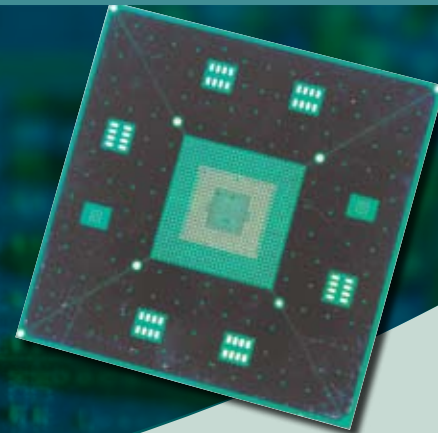


# CoreEZ™

## Thin Core FC Technology



### Thin Core FC Technology

El's CoreEZ™ semiconductor package utilizes the HyperBGA® manufacturing platform to offer a thin core build-up flip chip package with very dense core vias using a cost sensitive material set. The core via density provides 199 micron via-to-via core pitch resulting in an essentially coreless structure. High core via density is achieved using smaller pads and the same 50 micron laser drilled holes used in producing HyperBGA® to unblock wiring channels through the core. This enables CoreEZ™ to provide up to 2 times the number of signal layers as a standard build-up package that uses mechanically drilled core vias with large capture pads. The end result is an extremely cost effective solution that allows full strip line signal layers on both sides of the core.

Component cost is further reduced by enabling die shrink through die pad pitch reduction down to 150 microns. In addition, the thinness of the core provides improved power distribution and the ability to dissipate chip thermal power into the PCB. CoreEZ™ is an excellent choice for applications requiring low cost build-up materials along with high reliability, performance and wireability. It is also nicely suited to aerospace applications requiring radiation tolerance.

### Features

199 micron core via pitch,  
50 micron laser drilled vias

25 micron LW/LS

2X the board level reliability of a  
standard FC PBGA or FC ceramic BGA

Full signal wiring on both sides of core

Thin core (200 micron) reduces  
inductance

6, 8, 10 and 12 layers

Up to 4 full strip line signal layers

Low cost material set

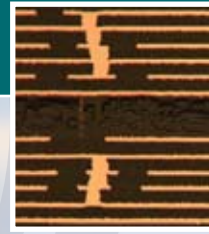
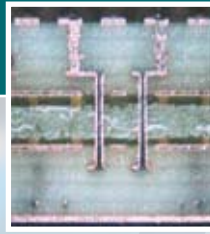
Thin core build-up

High speed differential pair designs

Parts available in any shape, enabling  
the merger of dense circuitization  
found in chip packaging with  
configuration variety found in  
traditional PCB technology

the power of innovation

# CoreEZ™ Specifications



Organic, thin core build-up flip chip technology that combines exceptional electrical, reliability and wireability performance with a cost sensitive material set.

## Specifications

### Laminate Features

Line width	25µm minimum
Line space	25µm minimum
Pad diameter	100µm minimum
Via diameter	50µm minimum (UV laser drilled)
Minimum die pad pitch	150µm die pad pitch
Build-up dielectric thickness	35µm, 50µm

### Materials

All planes	Copper
Dielectrics	P-Aramid in core and silica filled high Tg epoxy resin coated copper
FCA pad metallurgy	Coined solder bumps on copper, or on 200 microinches of e Ni on 4 microinches I Au on copper
Lid metallurgy/thickness	Copper/1mm (substrates do not include lids)

### Electrical Characteristics

Build-up layer dielectric constant	3.7 up to 2.5GHz
Build-up layer loss	0.013 at 1MHz
Core material dielectric constant	3.7 up to 2.5GHz
Core material dielectric loss	0.018 at 1MHz

### Physical Attributes

Single chip body sizes	JEDEC up to 55mm
System-in-package body sizes	Custom
Number of I/Os	Up to 2916 at 1.0mm BGA pitch
Die size	Over 18mm
Flip chip pad pitch	Down to 150µm
BGA pitch	0.50mm up to 1.27mm
Decoupling capacitors	Flip chip and SMT

### Reliability Stress Testing

Board level thermal cycles	Over 4000 cycles of 0° to 100°C
High-temperature storage	150°C for 1000 hours
Component level thermal cycles	1000 cycles of -55° to 125°C

Results may vary with different die, assembly processing or design attributes.

Test results for a 42.5mm body size with a 17.3mm die and 200µm die pad pitch with low melt bumps and a 42.5mm body size with a 14.7mm die and 225µm die pad pitch with high melt bumps.

For more detailed information about our CoreEZ™ technology, call us today at 866-820-4820. Our application engineers are ready to assist you with detailed information for successful product usage. You can also visit our website at [www.endicottinterconnect.com](http://www.endicottinterconnect.com).



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