

Manufacture and Ultra-High Frequency Performance of an LCP-based, Z-interconnect, Flip-Chip Package

Michael J. Rowlands, Rabindra N. Das
EI (Endicott Interconnect Technologies Inc.)
1093 Clark Street, Endicott, NY 13760
michael.rowlands@eitny.com, 607.755.5143, fax 755.6151

Abstract

We have designed and built a LCP-based flip-chip package using Z-interconnect building blocks for reliability and electrical performance. Manufacturing a Z-interconnect substrate involves building mini-substrates (sub-composites) of 2 or 3 layers each, then assembling several mini-substrates together to make the finished product. “Z-interconnect” is used to connect metal layers vertically, using a conductive adhesive. Z-axis interconnection was achieved using joining cores. Through holes in the joining cores, formed by laser drilling and having diameters 60 microns, were filled with an optimized, electrically conductive adhesive. The adhesive-filled joining cores were laminated with circuitized sub-composites to produce a composite structure. High temperature lamination was used to cure the adhesive in the composite and provide Z-interconnection among the circuitized sub-composites. Designing and manufacturing the mini-substrates separately makes it possible to reliably manufacture substrates with no via stubs, very low-loss materials, nearly arbitrary transmission line structures and lots of flexibility to tune features to reduce signal loss. Here we are using 5 sub-composites with 16 metal layers, including 3 OS2P joining cores, 2 2S2P signals cores, plated copper on top and bottom and embedded resistance on layer 7. Each sub-composite (OS2P/2S2P) made with high and low malting point LCP. There was no de-lamination of conductive adhesive filled LCP samples after pressure cooker test (PCT), and solder shock. Evaluation criteria for the test vehicle will include its ability to perform as a reliable, manufacturable, high-performance substrate. Results will be compared to typical ceramic and PTFE chip packages and the improvements over ceramic will be noted.

1. Introduction

The needs of the semiconductor marketplace continue to drive density into semiconductor packages. The high end of this market appears to be standard Application-Specific Integrated Circuits (ASICs), structured ASICs, and Field-Programmable Gate Arrays (FPGAs). These devices continue to need increasing signal, power, and ground die pads, and a corresponding decrease in pad pitch is required to maintain reasonable die sizes. The combination of these two needs is pushing complex semiconductor packaging designs. Traditionally, greater wiring densities are achieved by reducing the dimensions of vias, lines, and spaces, increasing the number of wiring layers, and utilizing blind and buried vias. However, each of these approaches possess inherent limitations, for example those related to drilling and plating of high aspect ratio vias, reduced conductance of narrow circuit lines, and increased cost of fabrication related to additional wiring layers. One method of extending wiring density beyond the limits imposed by these approaches is a strategy that

allows for metal-to-metal z-axis interconnection of sub-composites during lamination to form a composite structure [1-5]. Conductive joints can be formed during lamination using an electrically conductive adhesive. As a result, one is able to fabricate structures with vertically-terminated vias of arbitrary depth. Replacement of conventional plated through holes with vertically-terminated vias opens up additional wiring channels on layers above and below the terminated vias and eliminates via stubs which cause reflective signal loss [6,7].

More and more substrate designs require signals paths that can handle multi-gigahertz frequencies. The challenges for organic substrates, in meeting these electrical requirements, include using high-speed, low-loss materials, manufacturing precise structures and making a reliable finished product. In addition, many high-speed chip packages have mechanical and environmental requirements like lightweight and low-moisture absorption. One material that meets all of these requirements is a Liquid Crystal Polymer (LCP) dielectric which has unique combination of features and performance [8]. Due to its design flexibility, lighter weight and especially hermeticity, LCP-based Z-interconnect has potential to be a favorable alternative to low temperature co-fired ceramic (LTCC) substrates. In addition, the lower dielectric constant of LCP can reduce crosstalk and noise coupling compared to LTCC. **Figure 1** shows advantages of LCP structures.

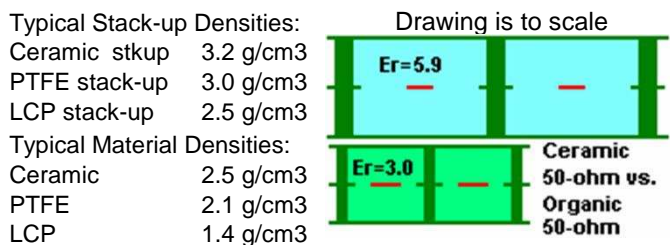


Figure 1 Advantages of LCP: Lightweight, High Signal Density

In the present paper, we design liquid crystal polymer (LCP) based test vehicle (TV) using the Z-interconnect building blocks, to make new RF structures. The work was involved to optimize dielectric and conducting adhesive materials for the structures. High and low malting point LCP based sub-composites Overall, this effort is an integrated approach centering on three interrelated fronts: (1) materials optimization, (2) fabrication, and (3) electrical performances at the package level.

2. Experimental Procedure

Z-interconnect Construction

The name “Z-interconnect” is short for Z-axis interconnect. Conductive, adhesive paste is used to connect thin substrates together, enabling versatile stack-ups that eliminate via stubs. This construction allows vias to start and stop on any layer. In addition, designs can be made with Z-interconnect, that include controlled impedance transmission lines with a range of line widths from narrow to very wide. **Figure 2** shows an example stack-up with various line widths and signals types and with no via stubs [5].

Red = RF signals Gray = all other signals

Purple = digital Dk Gray = Z-interconnect joints

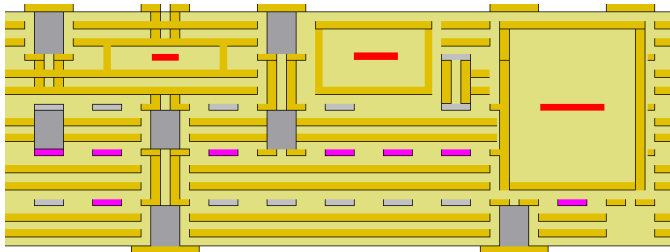
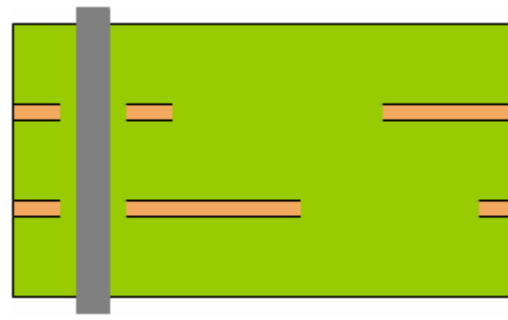
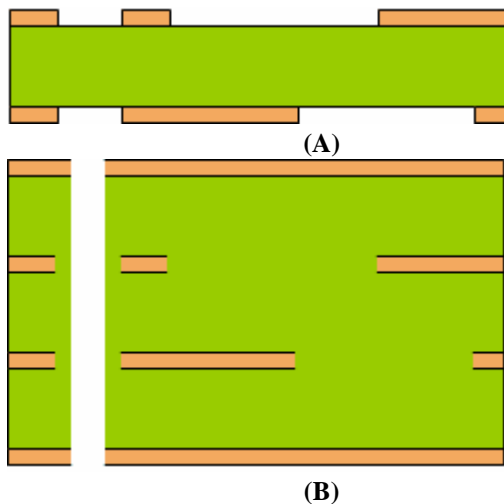


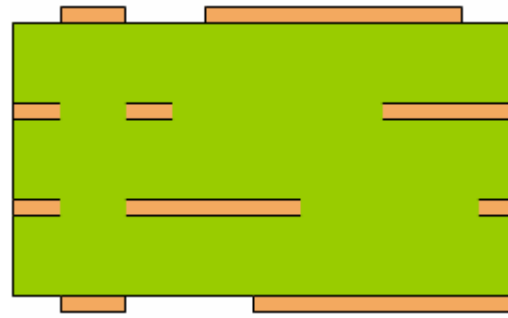
Figure 2 LCP Z-interconnect Stack-up

The general methods and processes used to build a Z-interconnect substrate are described in previous papers [2,5]. A summary is shown below highlighting the LCP material.

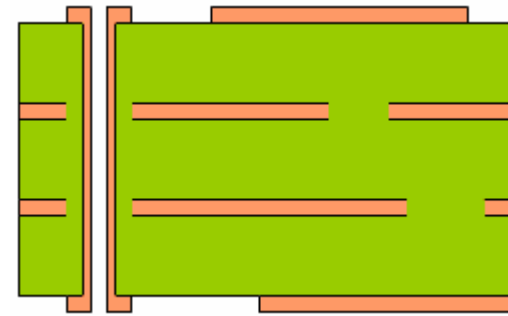
The main building blocks are a plane-plane (0S2P) core and a signal-plane-plane-signal core (2S2P). The joining core is the name of the 0S2P because it has a conductive paste which allows it to attach to the 2S2P signal cores. The joining core starts with an off-the-shelf copper-clad laminate. Then shapes and lines are etched into the copper on both sides. A layer of dielectric and copper is laminated to both sides of the etched plane-plane core and then holes are drilled through the structure. Lastly, the hole is filled with conductive paste and the outer copper is etched away, yielding a 0S2P joining core. These steps are sketched in **Figure 3A-C**.



(C)



(D)



(E)

Figure 3: Fabrication of joining and signal cores (A) Etch 2P core; (B) Drill laminated 2P core; (C) Paste fill drilled 2P core; (D) Etch laminated 2P core (E) Drill and plate laminated 2P core

The 2S2P signal core process starts the same as the 0S2P core, up to attaching the dielectric and metal layers to the 2P core. At the next step, instead of drilling, the outer copper is etched to create all the signal features. Lastly, the holes are drilled and plated to make the 2S2P core (**Figure 3D,E**). The 0S2P and 2S2P building-blocks are combined to make a Z-interconnect stack-up (see **Figure 4**).

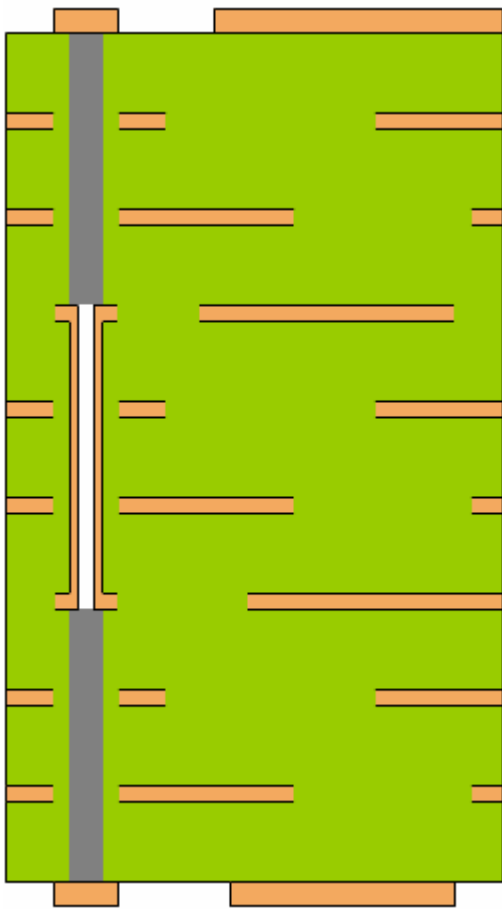


Figure 4: Z-interconnect composite stack-up

In combination with blind and buried vias (**Figure 5**), the signal and joining core building blocks allow arbitrary via connections starting at any layer and ending at any layer.

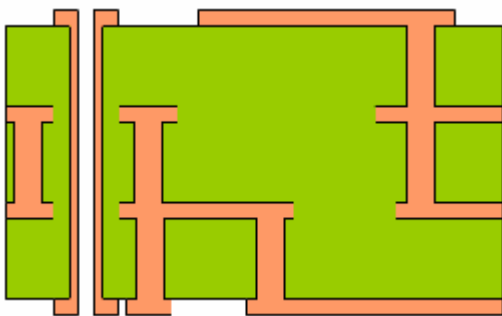


Figure 5: Buried and blind vias in core

Discrete embedded capacitors and resistors can be added to most layers in the stack-up. Barium titanate-fluoropolymer can be used for embedded capacitance layers [9]. Printable barium titanate nano-composites or thick film resistors or resistor foil are typically used for discrete embedded passives [10]. (**Figure 6**)

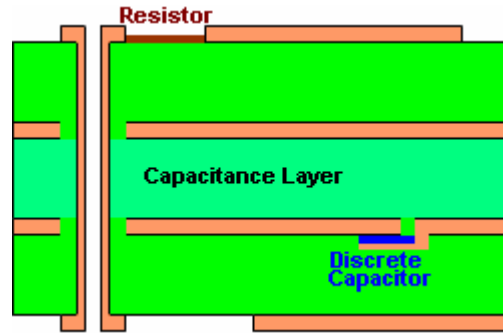


Figure 6: Embedded capacitance layer and embedded discrete caps and resistors

Test Vehicle Design

Test vehicles were designed using Z-interconnect building blocks. The main features, of the design, were 50-ohm RF structures in a range of line widths. Stripline structures were design using both narrow and very wide lines, ~50um and ~300um respectively. Co-planar structures were also designed using approximately the same narrow and wide line widths. Transmission line structures are shown in **Figure 7**.

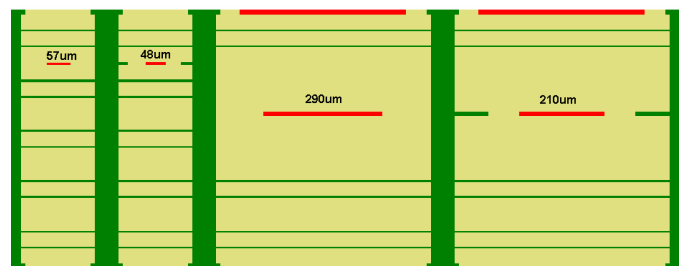


Figure 7: Test Vehicle Transmission Line Structures

In order to achieve these structures in this stack-up, 16 metal layers were used, including 3 0S2P joining cores, 2 2S2P signals cores, plated copper on top and bottom and embedded resistance on layer 7. Each dielectric layer was about 50um (2mils) thick. The stack-up used all LCP dielectric materials, combining copper-clad laminates and bond-films to achieve the final stack-up (see **Figure 8**). The total thickness of the stack-up was slightly less than 1mm. LCP dielectric specifications are $D_k = 2.9$ and $\tan\delta = .0025$.

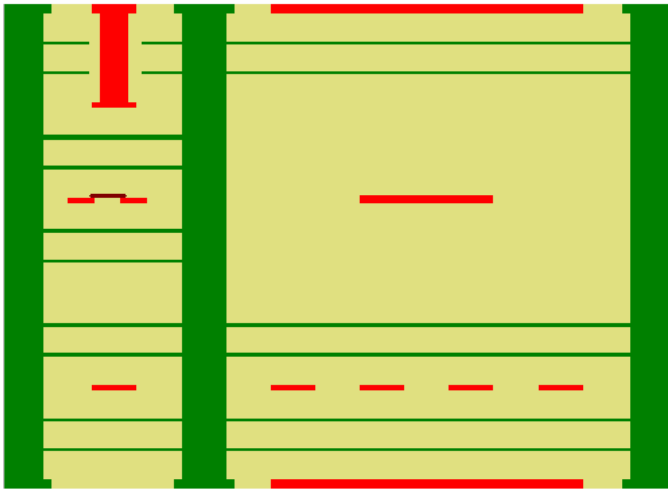


Figure 8: LCP Dielectric Final Full Stack-up

3. Results and Discussion

All-LCP z-interconnect test vehicle has a few big challenges. The challenges include processing LCP in a sub-composite, forming a good conductive paste connection and filling clearances during lamination steps. Sub-composites were successfully built after developing optimum process parameters. As a thermoplastic material, LCP requires a narrow range of temperature and pressure to laminate properly. **Figure 9** shows a LCP sub-composite panel.

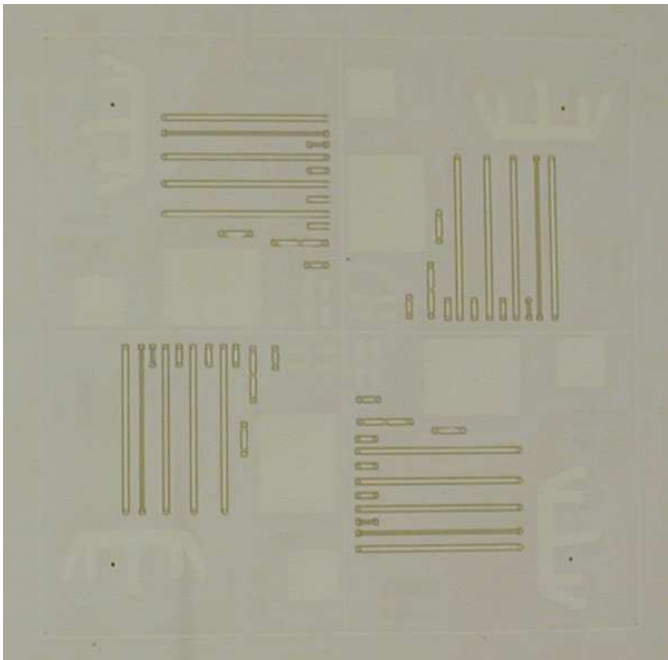
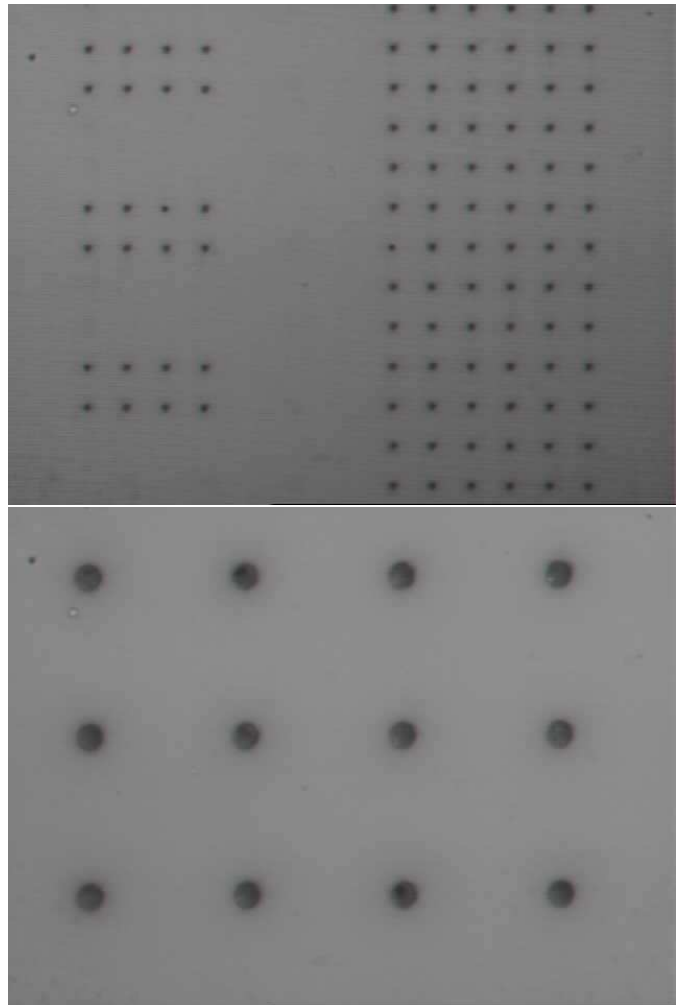


Figure 9: LCP Sub-composite Panel

The second building block in this LCP study is a 0S/2P core. This core is constructed using a high temperature melting LCP power core, sandwiched between layers of low melting LCP material. Through holes in the core are filled with an electrically conductive adhesive. By alternating 2S/2P and 0S/2P cores in the lay-up prior to lamination, the

conductive paste electrically connects copper pads on the 2S/2P cores that reside on either side of the 0S/2P core. Two signal layers are added to the composite structure each time one adds an additional 2S/2P core and an additional 0S/2P core. A structure with four signal layers composed of five sub-composites (two 2S/1P cores and three 0S/1P cores) is shown schematically in **Figure 2**. Although this particular construction comprises alternating 2S/2P and 0S/2P cores, it is possible to place multiple 0S/2P cores adjacent to each other in the stack. The adhesive-filled joining cores were laminated with circuitized sub-composites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide Z-interconnection among the circuitized sub-composites. Photographs show an adhesive-filled 0S/2P joining core prior to lamination. **Figure 10** shows optical photographs of a joining core having paste-filled holes with a diameter of 60 μm . Paste joints were formed using conductive paste. Paste formed a bond with metal pads on sub-composites above and below the joining core. **Figure 11** shows a completed Paste joint connecting ground planes together.



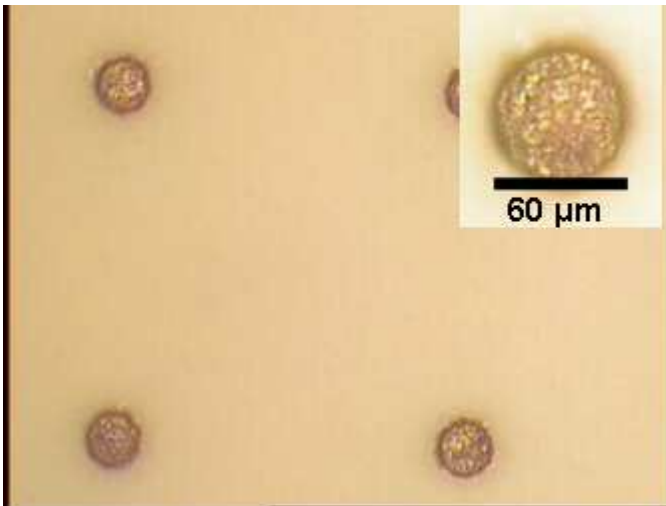


Figure 10: Photographs of adhesive filled joining core prior to lamination.

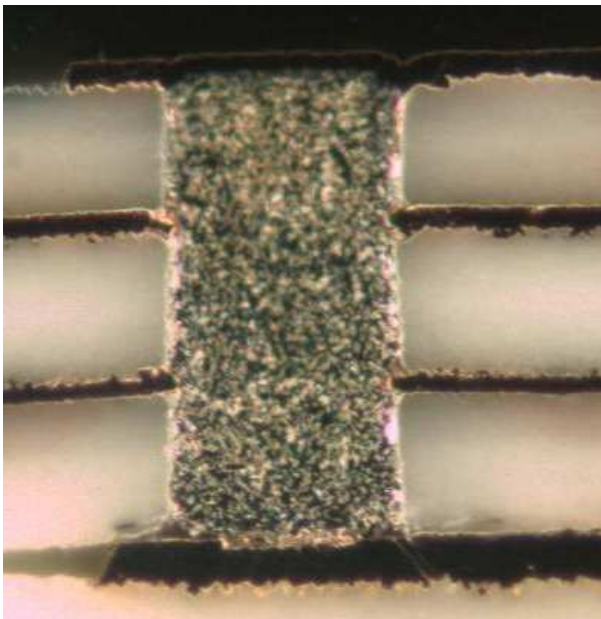


Figure 11: Conductive paste joint in LCP parts.

Work is continuing in optimizing a process for final lamination of the sub-composites. Sometimes, during final lamination, excess flow of LCP material cause de-lamination and buckling in some layers. **Figure 12** shows cross section of chip carrier taken from different area. It shows most of area has maintained well laminated stack-up except a couple of layers.

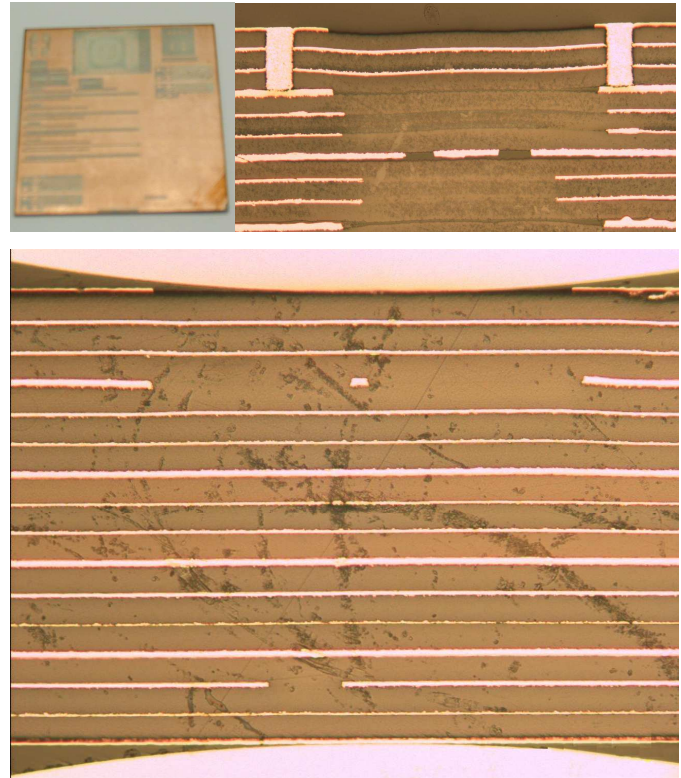


Figure 12: Cross-section of Final LCP Stack-up (inset: top view)

A similar test vehicle with Teflon-based material contains the wide transmission-line structures shows very low-loss. **Figure 13** shows insertion loss for a 1.1" stripline, line width 270um.

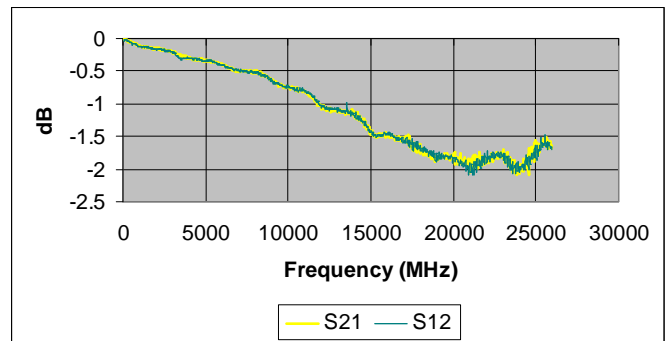


Figure 13 : 270um Width Transmission Line loss for Teflon based TV(similar results expected for LCP TVs)

Conductive adhesives are of little value unless they can survive the same rigors of testing that modules or boards would receive. Multilayer LCP laminate and adhesive filled multilayer LCP laminate was used for reliability testing. Reliability of the laminate was ascertained by PCT and solder shock. For PCT, samples were exposed to 100% humidity with a constant pressure of 19 PSI at 121 °C. Samples were stable after reliability test and there was no de-lamination after PCT and solder shock. Laminates were also exposed to PCT (2 hrs) followed by a 15 seconds solder dip at 260 °C.

Sometimes PCT and solder shock cause de-lamination. In general, solder dip/shock pick up the PCT defects and induce de-lamination. Here de-lamination propagates through the LCP, not through the adhesive.

4. Conclusions

LCP sub-composites were built successfully. Conductive paste filled the appropriate drill hole and formed a strong conductive, adhesive bond. Final lamination of LCP sub-composites requires specific processes and tight control of temperature and pressure. Optimization of LCP final lamination is ongoing.

Z-interconnect substrate structures with low-loss organic materials such as Teflon, have electrical loss performance that compares favorably to LTCC. **Figure 14** shows loss of a 270um width transmission line in a Teflon-based dielectric material. Analysis and simulation of LCP-based substrates predict that LCP structures will be even lower loss than Teflon. [6,7,11]

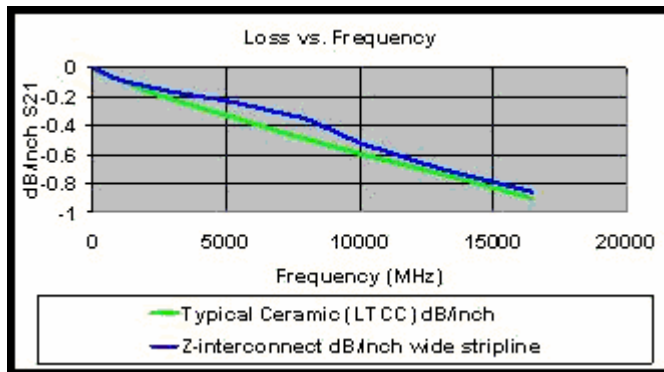


Figure 14 Teflon Z-interconnect Comparison to Ceramic

4. Conclusions

LCP based Z-interconnect substrate, with large clearances in planes and embedded resistors, can be built with sufficient flatness on subsequent metal layers. Using 0S2P and 2S2P building blocks, a nearly arbitrary stack-up of signals and planes can be built. High aspect ratio, small diameter (~60 μm) holes were successfully filled with silver-filled adhesives. Conductive joints were stable after pressure cooker test (PCT), and solder shock. The adhesive-filled joining cores were laminated with circuitized sub-composites to produce a composite structure. High temperature lamination was used to cure the adhesive in the composite and provide stable, reliable Z-interconnections among the circuitized sub-composites.

Future work involves optimizing a process for laminating multiple LCP sub-composites. Additional steps include electrical testing of a full LCP stack-up and mechanical and reliability tests.

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