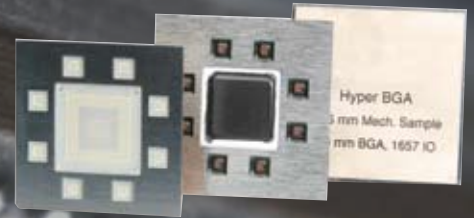
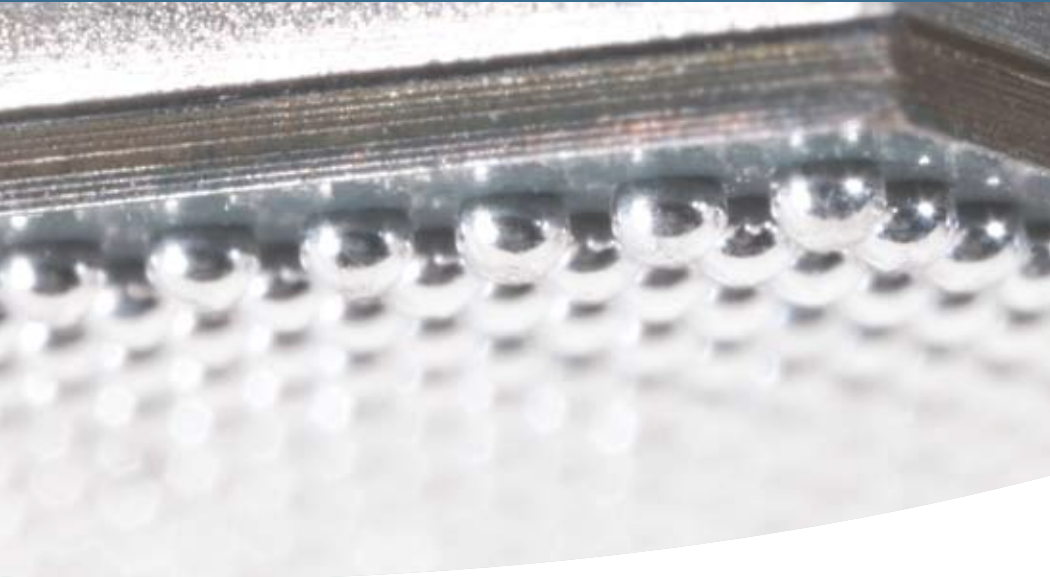


HyperBGA[®] Technology



Features

Outstanding SiP solution offers longest overall board level flip chip BGA life available

Delivers 2–10 times the flip chip BGA package reliability over ceramic BGAs

Assembled using standard SMT processes and materials; columns or land grid array sockets are unnecessary

Full strip line structures

Low coupled noise

Low weight

Very low power distribution inductance

Great SiP solution capable of flip chip, SMT or CSP component attach on both sides

Compliant laminate minimizes die and BGA stress when using large die and large body sizes

Substrate engineered to balance the CTE mismatch between silicon and printed circuit board for high reliability

Voltage plane splits provide the ability to turn on/off a higher number of selected die areas for improved power consumption and noise control

Thin, low profile fits easily in tight board-to-board spaces

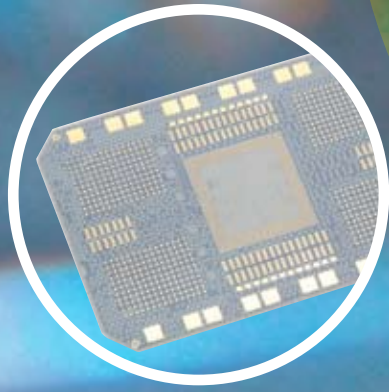
Parts available in any shape, enabling the merger of dense circuitization found in chip packaging with configuration variety found in traditional PCB technology

High speed, outstanding reliability

El's HyperBGA[®] flouropolymer-based coreless semiconductor package allows your die to run at extremely high rates of speed. The combination of the low loss, low dielectric constant material and strip line cross sections enable signal speeds surpassing 12 Gb/s. The material compliance of the PTFE, combined with the dimensional stability of a copper-invar-copper center plane, enables HyperBGA[®] to provide long field life, with none of the BGA wear out, die cracking, delamination or flip chip bump fatigue other packages exhibit.

The HyperBGA[®] product line is a great solution for networking, high end server, telecommunications, military and medical markets where speed, reliability and increased signal I/O, along with reduced weight, height and overall package size are critical. This low stress flip chip laminate package is also ideally suited to graphics applications that require high data processing speeds or any application requiring a system-in-package (SiP) approach.

the power of technology



The HyperBGA® semiconductor package is a PTFE-based organic flip chip designed to meet the needs of high performance applications

Specifications	
Laminate Features	
Line width	25µm minimum in die area
Line space	30µm minimum in die area
Via diameter	50µm minimum (UV laser drilled)
Layers	Up to 11
Materials	
Ground plane	Copper-invar-copper
Outer dielectric	Epoxy (APPE)
Flip chip metallurgy	Coined 63/37 eutectic on copper or on 200 microinches of e Ni on 4 microinches I Au on copper; lead free
BGA metallurgy	Presolder on copper, OSP on copper or on 200 microinches of e Ni on 4 microinches I Au on copper; lead free
Common Electrical Characteristics	
Time of flight	5.6ps/mm
Controlled impedance (Zo)	50–60 Ohms
Cross talk (Vne)	<15%
Power/ground loop inductance	5–10pH
Dielectric constant	2.7 at 1MHz
Dielectric loss tangent	0.003 at 1MHz
Physical Attributes	
Body sizes	JEDEC, 17mm–55mm
SiP body sizes	Custom
Number of BGA I/Os	Up to 2916 at 1mm pitch
Die size	>18.3mm
BGA pitch	0.5mm–1.27mm
Decoupling capacitors	Flip chip and SMT
Reliability	
Moisture sensitivity	JEDEC Level 3
Board level thermal cycles	10,000 cycles of 0° to 100°C
High-temperature storage	1000 hours at 150°C
Component level thermal cycles	1000 cycles of -55° to 125°C
HAST	264 hours of 110°C/85% RH/3.7V
Pressure pot	96 hours at 121°C/100% RH/2 ATM
Temperature, humidity, bias	1000 hours at 85°C/85% RH/3.7V
.....	
Results can vary with different die, assembly processing and design attributes	

For more detailed information about our HyperBGA® technology, call us today at 866-820-4820. Our application engineers are ready to assist you with detailed information for successful product usage. You can also visit our website at www.endicottinterconnect.com.



1093 Clark Street Endicott, New York 13760 Phone: 866-820-4820 Fax: 607-755-7000
 For more information, visit our website at www.endicottinterconnect.com