

Migrating Printed Wiring Board Assemblies into System in a Package (SiP)

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Abstract

The demand for system miniaturization in many applications has led to efforts to put all or most of the functions on a single chip. However, there are many situations where this is not possible or cost prohibitive. Memory uses large amounts of chip area and several different memory types may be needed to fulfill the functional requirements. In many cases, the need for analog and digital functions may make consolidation on a single chip impossible. An alternate approach is to preserve the proven functional design and miniaturize at the package level to achieve the desired space savings. The approaches explored in this publication include eliminating active chip packages by directly attaching the chip to the SiP with flip chip technology. Additionally, the area devoted to passive components can be greatly reduced by embedding many of the capacitors and resistors. In some instances, the connector systems that were consuming large amounts of space in the traditional Printed Wiring Board (PWB) assembly can be reduced with a small pitch connector system. This PWB assembly can then be transformed into a much smaller SiP with the full surface area on both sides of the package effectively utilized by active and passive components. A further benefit of the SiP is a major reduction in total height. Two specific cases will be detailed and the size reductions shown. The concept of a SiP index will be introduced to show how the SiP area compares to active die area. The miniaturized SiP with its reduced package size and demand for passives requires a high wireability package with embedded passives and excellent communication from top to bottom. Endicott Interconnect Technologies has a Core EZTM package that meets these requirements. The details of the package design parameters and package electrical performance are demonstrated.

Key words: package, miniaturization, assemblies, system, MCM, embedded passives

Introduction – PWB Assemblies – Candidates to Migrate to SiP

Tradition PWB assemblies logically integrate a variety of functions to achieve an end result that will communicate to the rest of the system. These components are complemented by passives, mainly resistors and capacitors, to achieve desired waveforms and filter out electrical noise due to circuit switching. Since the advent of Surface Mount Technology (SMT), most components can be assembled directly to pads on the surfaces of the PWB. In order to keep the total height down and ease assembly, typical designs have most active components on one surface which we will call the top surface and passive components on the opposite surface which will be called the bottom surface. The assembled PWB top surface is typically more completely populated than the bottom and this unbalance leads to a larger area for the product

than would have been achieved with a totally balanced placement of components on the two sides. However, the totally balanced placement would result in a much thicker assembled PWB and have significant system impact. Therefore, our base point for this study is a PWB with active components and connectors on the top and passives on the bottom. Two different designs are quantified; Example A and Example B. Both have a mixture of analog and digital active circuits which makes integration into a single chip extremely difficult. In both cases, a variety of individual functions are represented in the digital active components further discouraging chip integration. The distribution of active components, passive components and connectors for these two cases is shown in Table 1.

Table 1 - Component Counts for Examples A and B

	Total Components	Active Components	Passive Components	Connectors
Example A	310	17	277	16
Example B	705	49	655	1

Example B is a more efficient PWB assembly because the connectors have already been integrated and the passives in Example B have been miniaturized. In Example A, there was little motivation to miniaturize the passives because the back side had more than enough room to handle the passives without miniaturization.

When these assemblies are redesigned into a SiP, the component count drops significantly with Example A dropping to 99 components and Example B dropping to 136 components; a 3x to 5x reduction. The area reduction is even more dramatic; 8x to 9x. Since the SiP has eliminated all the very tall components, the total height is reduced and the volume reduction is 17x to 21x. The next sections will show the technologies that enabled these improvements and quantify the gain achieved with each element.

SiP Features for Size Reduction

The SiP has four features that can significantly reduce the size of the final assembly. The first is to remove the active components from their package and assemble them directly to the SiP. The most efficient approach is to use Flip Chip Assembly (FCA). Many components have not been designed for FCA but if desired they can be converted to make FCA possible. The approaches to achieve this will be described. The second key item is to embed into the PWB as many of the passive components as possible. Resistors with values ranging from 15 ohms to 30,000 ohms can be efficiently embedded. Capacitors that are used for noise suppression (bypass / decoupling) and have values up to 0.1 microfarads (uf) can also be embedded. The SiPs described here will use a Passive Core that incorporates both the resistors and capacitors. The third key item is balancing the component area on both the top and bottom layers. With many passives eliminated and the active components in FCA format, components can be freely placed on top or bottom with little impact on the total height of the SiP assembly. The fourth item is efficiently using connector area. A fine pitch connector that is placed near the edge of the part minimizes the loss of functional area.

FCA

Components that use Flip Chip (FC) Packaging are the easiest to accommodate and can be shipped to the

SiP assembly site after dicing. If the chip was meant to be assembled to the package with wire bonding, there are two approaches that can make them compatible with FCA. Stud Bumping [1] [2] with solder reflow can be utilized if the pad pitch on the chip is large. A good rule of thumb for Stud Bumping with solder reflow is a minimum pitch of 115 um between pads. The stud bump is equivalent to applying a wire bond (gold or copper) to the chip pad and then shearing off the wire. Typical size of the bump is 50 um diameter and 75 um high. Figure 1 shows a top view of chip pads with stud bumps applied and ready for assembly.

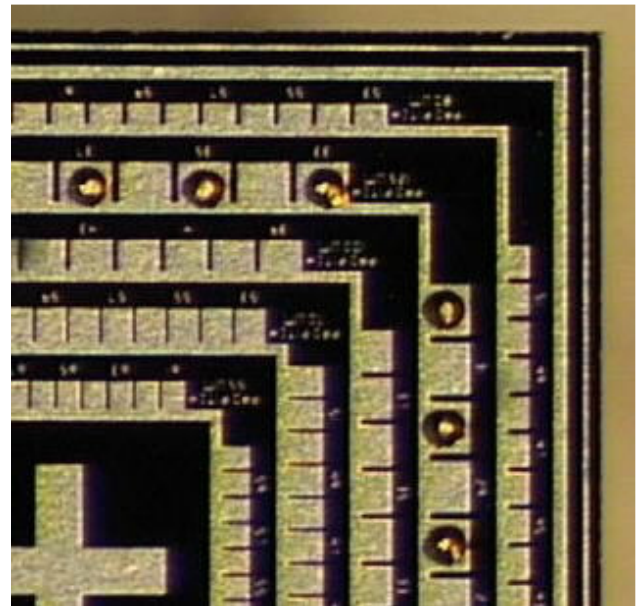


Figure 1 - Stud Bumps on Chip

The solder supply on the substrate is used to connect to the stud bump and concern for solder bridging limits the minimum pitch for this approach. The second approach is to redistribute the pads on the top surface of the chip into a pattern that uses typical Flip Chip technology. This is achieved with one or two thin film layers using semiconductor materials such as polyimide insulation and aluminum-copper conductors. The top surface then has a solder bump applied in the same manner as a chip intended for Flip Chip assembly. This approach is not limited by pad pitch and is the preferred approach for high volume production. However, the investment in design, wafer masks and wafer purchase makes the cost prohibitive for prototypes. Therefore, the wire

bond chips for the prototypes may have a mixture of stud bump and redistributed chips with the intention to have all the chips redistributed for the production phase. The significant reduction in area consumed by the active components, about 7x, is achieved by converting from Packaged parts to Flip Chip as noted in Table 2. In all cases, assembly required spacing was included in the component areas.

Table 2 - Area Comparison for Active Components- Packaged vs. Flip Chip

	PWB Packaged Component Area (sq mm)	SiP Flip Chip Die Area (sq mm)	Area Reduction Ratio
Example A	3598	495	7.3
Example B	13,222	1,989	6.6

Passives

Capacitors, resistors and inductors represent the majority of the component count on these assemblies.

The inductors were left in component format since there are a small number of them and integrating them into a package would not be efficient. Many of the capacitors are used for bypass or power supply decoupling and are fairly low in value. Capacitance material capable of providing 50 nanofarads (nf) per square inch has been proven feasible [3]. When the capacitor is embedded in the substrate, the impedance from the active device to the supporting capacitor can be much lower than with a discrete SMT capacitor. Therefore, a much lower capacitor value can provide the required filtering. The designs shown here use a 40x factor for effectiveness of embedded capacitance vs. discrete SMT capacitors based upon embedded capacitance results reported to the industry [4]. Example A requires 4.6 embedded layers to replace 9.1 uf of discrete capacitance. Example B requires 2.9 layers to replace 25.7 uf of discrete capacitance. The passive core technology (Fig. 2) developed by Endicott Interconnect Technologies is capable of providing up to 6 layers of embedded capacitance and could be extended further. Table 3 shows the impact on component count and area by embedding capacitors up to a value of 0.1 uf in the SiP.

Via Structures	Layer	CoreEZ Thin Build-Up 3-8-3	Estimated Thickness (um)	Potential Function
Stacked (if needed)	Top	Driklad Filled RCC	12	Mounting / Signal / Power
	2T	Driklad Filled RCC	12	Signal / Power
	1T	Driklad Filled RCC	12	Signal / Power
		Driklad Filled RCC	34	
PTH	CL1	Embedded Capacitance	18	Power / Signal
	CL2	Embedded Capacitance	12	Power
	CL3	Embedded Capacitance	6	Power
	CL4	Embedded Resistance	12	Power / Resistance
		Thermount	110	
	CL5	Embedded Resistance	6	Power / Resistance
	CL6	Embedded Capacitance	12	Power
	CL7	Embedded Capacitance	6	Power
	CL8	Embedded Capacitance	12	Power
		CL8	Driklad Filled RCC	18
	1B	Driklad Filled RCC	34	Signal / Power
	2B	Driklad Filled RCC	12	Signal / Power
	Bottom	Driklad Filled RCC	32	Signal / Power
		Total	522	
		Core (Incl cu)	254	

Figure 2 - Cross - Section of SiP with Passive Core

Table 3 - Capacitor Count and Area Impact by Embedding Capacitors in SiP

	PWB Capacitor Count	SiP Capacitor Count	Capacitor Count Ratio	PWB Capacitor Area (sq mm)	SiP Capacitor Area (sq mm)	Capacitor Area Reduction Ratio
Example A	200	71	2.8	467	269	1.7
Example B	490	68	7.2	647	251	2.6

One notes that the area reduction ratio is lower than the component count ratio because the larger capacitors cannot be embedded.

The 40x factor was experimentally developed based on reconfigured systems performing acceptably in functional mode. It is a good starting point for assessing miniaturization feasibility. However, it is often necessary to characterize the impedance profile of the power delivery network (PDN) as a function of frequency. Required impedance and bandwidth are often known.

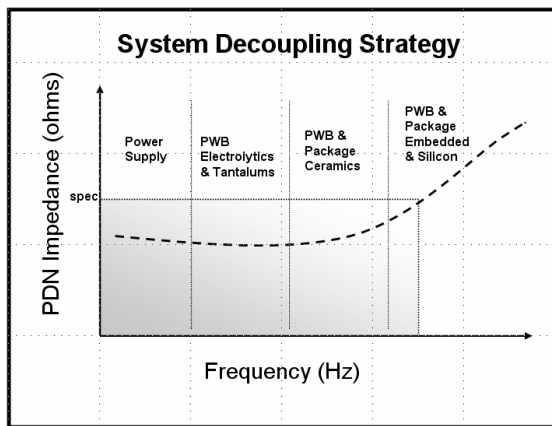


Figure 3 - System Decoupling Strategy

System decoupling, in the form of bypass capacitors on the PWB, package, and silicon, is then utilized to bring the PDN impedance within specification. Electrolytic bulk capacitors (high C) are often employed on the PWB to extend the bandwidth into the MHz range. Tantalum capacitors provide a mid-frequency boost and high frequency (low ESL) ceramic capacitors further extend the PDN bandwidth. The equivalent series inductance (ESL) of even these “high-frequency” SMT capacitors is still ineffective in the bandwidth beyond 1 GHz, even when many capacitors are placed in parallel to reduce the effective impedance.

Given the speeds of today’s IC’s, a PDN must supply more than voltage at DC. Figure 3 depicts a common system decoupling strategy. While a power supply will typically deliver voltage at low impedance, its bandwidth usually only extends to the KHz range.

The PDN can be characterized in the design phase by modeling with simulators such as Ansoft’s SIWave. It is possible to extract the complete PDN from the physical design database. This extraction can include all internal power planes, power vias, traces, embedded components, discrete components, and interconnect arrays for both die and PWB attach. Figure 4 shows a side view of a typical PDN extraction done in SIWave. Once this extraction is accomplished, s-parameters and impedance can be calculated directly and compared to the specification. This technique provides a more accurate determination of the potential to embed surface components and realize miniaturization.

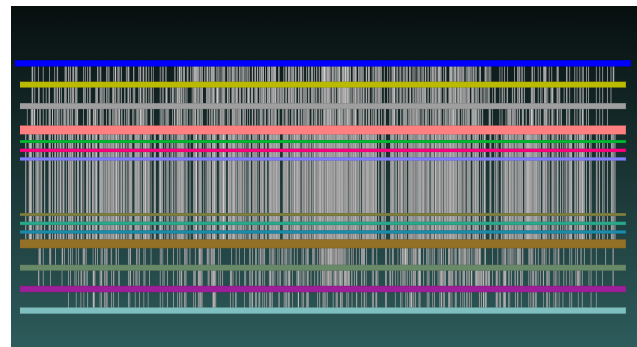


Figure 4 - PDN Extraction

Embedded capacitance tends to be most effective at higher frequencies. Given the constraints of the currently available embedded materials, the maximum capacitance density is usually not sufficient to provide significant bulk values of capacitance. Discrete SMT capacitors are still necessary for low and mid-frequency impedance reduction. Figure 5 shows simulated PDN impedance as a function of frequency for a one inch package. Four cases are examined; 1) with no decoupling capacitors, 2) with one decoupling capacitor, 3) with 201 decoupling capacitors and 4) with embedded capacitance and no decoupling capacitors. At higher frequencies, the inductive parasitics associated with SMT devices and their

termination become limiting. For this reason, large quantities of SMT decaps are often populated to reduce the effective inductance. This is counter-productive to system miniaturization. Due to the distributed nature of embedded capacitance, the inherent impedance and that associated with

connection are significantly lower than SMT devices. Therefore, replacing SMT decaps with embedded capacitance at 40:1 or a greater capacitor value ratio improves high frequency performance and miniaturizes the part at the same time.

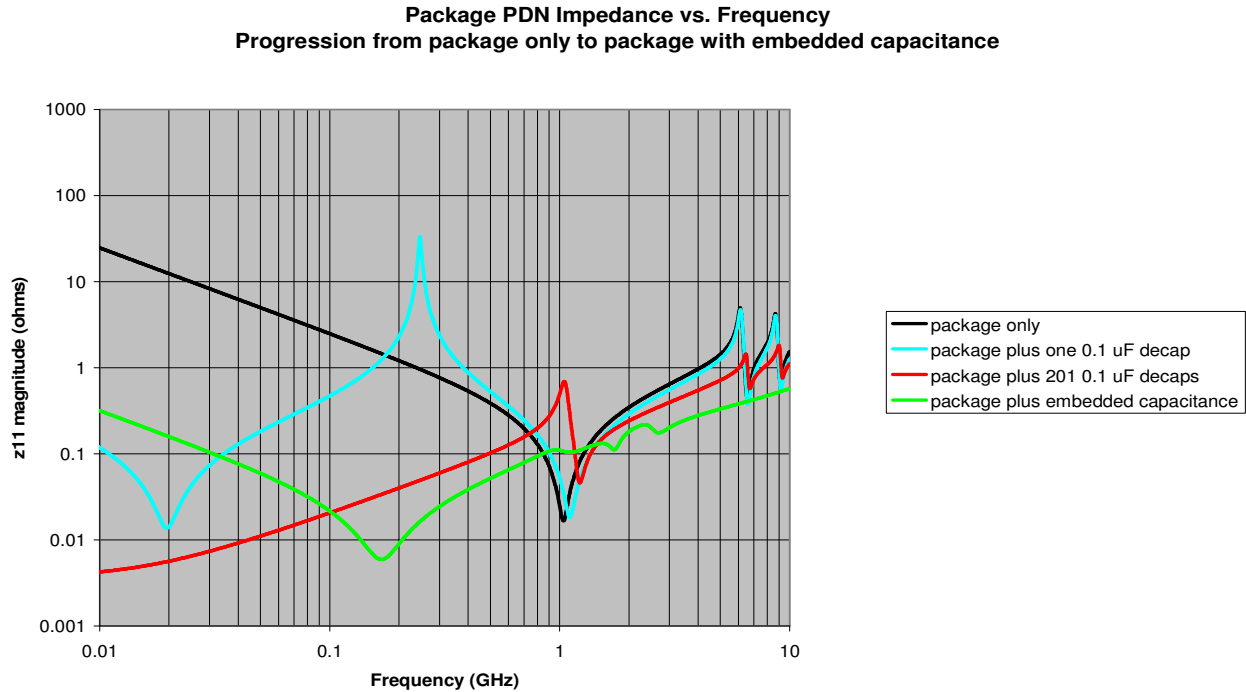


Figure 5 - PDN Impedance vs. Frequency as a Function of Capacitor Configuration

Embedded resistor technology can use either thin film materials that are applied on the copper foil or screened resistor material that can be applied at any level. The approach chosen in these examples is thin film material and it is incorporated into the center layer of the core. The top of the core uses 25 ohm per square material and the bottom of the core uses 250 ohm per square material. This combination enables resistor ranges from 15 ohms through 30,000 ohms with efficient sizes for the embedded resistors. The embedded resistors can be laser trimmed to a tolerance of 1% which is usually acceptable for most applications. Power is also a consideration and the embedded resistor area needs to be matched to the power requirement. In these examples, this is only a concern for low value resistors because the maximum voltage in these applications is about 3 volts and a resistor of 100 ohms or higher can only draw 0.09 watts which can be dissipated in a small resistor area.

Figure 6 shows a serpentine 10,000 ohm resistor using 250 ohm per square material. One of the features of the passive core is the use of Core EZ's fine pitch 50 um via diameter on a pitch as small as 200 um. This allows vias to be placed within the legs of the serpentine resistors as shown in Figure 6. The ability to provide a high density of vias through the resistor network is critical for both signal wiring density and the effectiveness of the capacitor layers. Table 4 shows the component count reduction and area reduction attributed to embedding resistors.

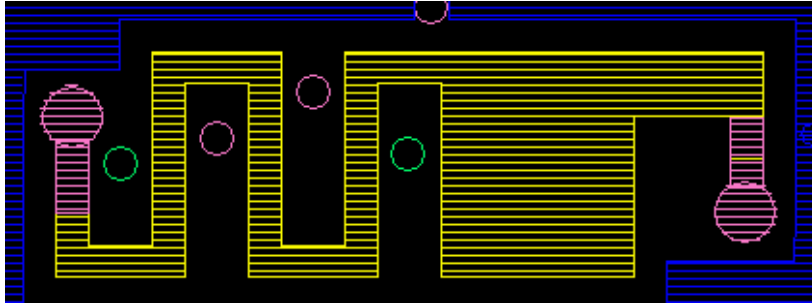


Figure 6 – Embedded Serpentine 10,000 Ohm Resistor with Vias in Legs – 1.0 mm x 3.3 mm

Table 4 - Resistor Count and Area Impact by Embedding Resistors in SiP

	PWB Resistor Count	SiP Resistor Count	Resistor Count Ratio	PWB Resistor Area (sq mm)	SiP Resistor Area (sq mm)	Resistor Area Reduction Ratio
Example A	70	3	23.3	137	8	16.7
Example B	151	18	8.4	143	17	8.5

Connectors

In example A, the use of multiple connectors contributed to significant area consumption which is not consistent with miniaturization. A single connector at 1 mm pitch between connections replaced the multiple connectors and reduced the connector area from 1614 sq mm to 308 sq mm; a 5.2x reduction in area. The single connector will most likely result in higher wiring demands and a SiP with good wiring capacity is required.

Double Sided Effectiveness

The elimination of large components through FCA and reduction in components through embedded passives eliminates concerns about total height of the assembled SiP and allows flexibility to fully use both sides of the SiP. Full double sided utilization saved 2510 sq mm in example A and saved 8265 sq mm in example B. Good double sided utilization can place a large demand on z-axis communication and a SiP with small holes in the core layer and ability to thread holes through the resistor legs enables an efficient double sided product.

SiP Index

One of the measures of the effectiveness of a package is the package area vs. the area that is consumed by active chips on the package. A SiP Index of 1.0 is achieved by a single chip. In Example A, the PWB version had a SiP Index of 11.5 which indicates a package significantly larger than the sum of the active chip area. The redesign of Example A into a SiP reduced the SiP Index to 1.3, very close to the

ideal of 1.0. Example B has a similar result. The SiP Index of the PWB version of Example B is 8.8, dropping to 1.1 in the SiP redesign.

Summary

Effective miniaturization requires a combination of changes which all interact to achieve the desired goals for a SiP. Large active components must be removed from their packages and assembled directly to the SiP. As many passive components as possible need to be embedded inside the SiP thereby relieving real estate on the surfaces and in many cases improving electrical performance. Connectors need to be consolidated. SiP wiring capacity must be high because component placement will be more concerned with real estate than with easy routing. The SiP must also have an ability to communicate efficiently in the z-direction to handle the double sided demands. The substrate shown in Figure 4 has both high wireability and high z-direction communication by use of 25 um lines, 50 um diameter Microvias and 50 um diameter PTHs. An overall summary of the final achievement of an area reduction of 8x to 9x and volume reduction of 17x to 25x is summarized in Table 5. This is illustrated to scale in Figures 7 and 8.

Table 5 – Summary of Area, Height and Volume Reduction with SiP vs. PWB

	PWB Area (sq mm)	SiP Area (sq mm)	Area Ratio	PWB Ht (mm)	SiP Ht (mm)	Ht Ratio	PWB Volume (cu mm)	SiP Volume (cu mm)	Volume Ratio
Example A	5715	632	9.0	6.8	2.5	2.7	38,863	1581	24.6
Example B	17,346	2253	7.7	6.5	3.0	2.2	113,332	6758	16.8

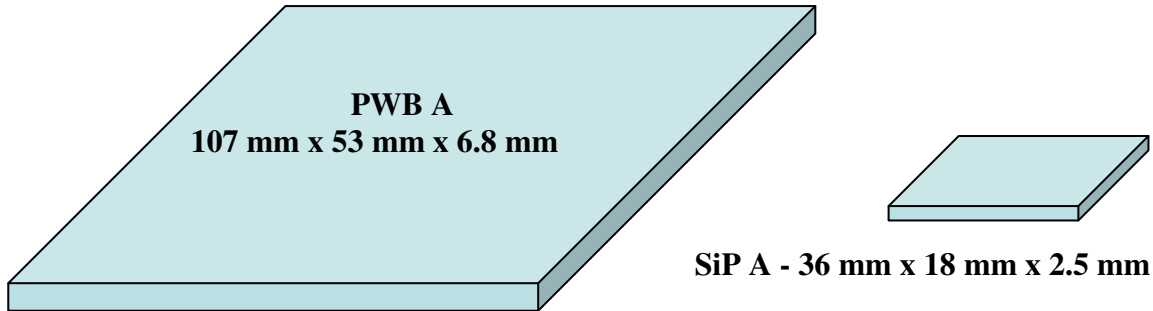


Figure 7 - Example A - PWB vs SiP

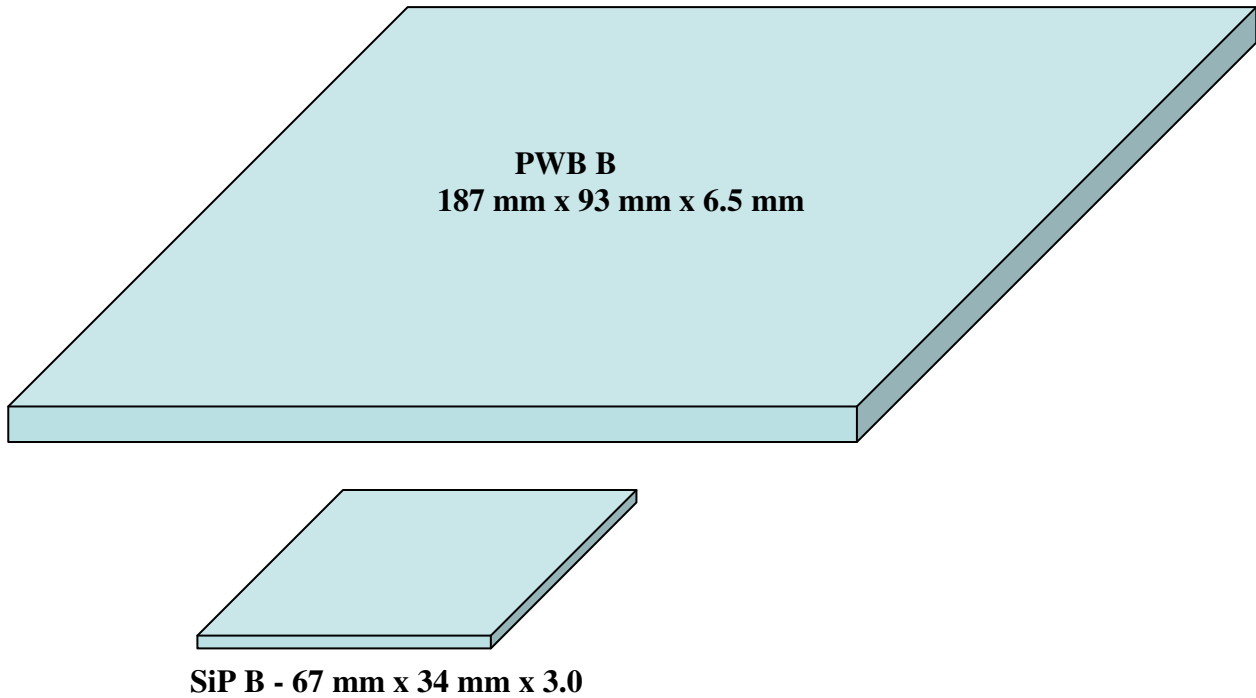


Figure 8 - Example B - PWB vs. SiP

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