Thermal Performance of a Thin High Interconnect Density Organic Substrate for Flip-Chip Applications

Varaprasad V. Calmidi
Endicott Interconnect Technologies, Inc.
1701, North Street, Endicott, NY 13760
Ph: (607) 755-1167
E-mail: vara@eitny.com

Abstract

The thermal performance of a thin (0.5mm), high interconnect density substrate for flip-chip applications (FC-PBGA) has been studied under natural and forced convection conditions per JEDEC standard conditions [14]. Since the effect of a heat sink not considered, heat conduction within the package and substrate is relatively more important to thermal performance. A package size of 42.5mm is assumed. The effect of die size, core vias in the substrate, and lid assembly conditions is studied. The lid assembly conditions have the greatest effect on theta-ja (up to 38%). The effect on theta-ja of increasing the number of core vias under the die site is also dependent on the lid assembly. When the lid is attached to a stiffener on the substrate, a negligible change (3%) in theta-ja is observed when the number of core vias is increased (i.e. increasing k_{zz} from 0.6 to 3.1 W/m-K). When a floating lid that is not physically coupled to the substrate is used, up to 9% difference is observed. These and other results are discussed in the light of various conduction heat flow paths within the package.

Nomenclature

A area
Cp heat capacity
g gravity vector
k thermal conductivity
k_{zz} effective out of plane conductivity of substrate (under die region)
p pressure
q^r heat transferred by radiation
s thickness of control volume
S^r radiation source term in energy eqn. (solids only)
t time
u velocity vector
P Power dissipation (W)
T Temperature (C). (K for radiation calculations)
T_j Chip temperature (C)
T_a Air temperature
<> fourth power average quantity

Symbols

ε emissivity
μ dynamic viscosity
ρ density
σ Stefan-Boltzmann constant
θ_{ja} Junction-to-ambient thermal resistance (C/W) = (Tj – Ta)/P

Introduction

Rapid improvements in chip technology are driving improvements to flip-chip packages that incorporate substrates with polymer based dielectrics. These packages are used in a variety of applications (e.g. ASIC, microprocessor, digital signal processing). Increasingly they have generated interest in System-in-Package and multi-chip applications [1], as well.

One type of flip-chip ball grid array packages (FC-PBGA) contain substrates with a "core" layer with through-via interconnections, and additional "build-up" layers for signal and power distribution/routing. Traditionally, these types of substrates have been limited in capability by core via diameter and pitch. However, recent advances in flip-chip bump pitch, electrical, and system-level requirements have increased demands on package wireability, electrical, thermal, and reliability performance. A new type of "thin-core" substrate, CoreEASEI™, has been developed to address these challenges (see [2] for advantages of high density cores). Some of the characteristics of CoreEASEI such as dense core via pitch, via size, particle filled dielectric, substrate thickness, and assembly conditions are expected to affect thermal performance.

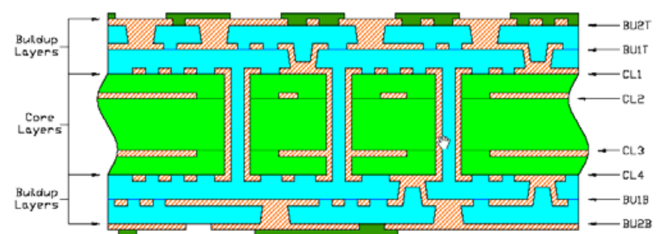

Figure 1 : Substrate cross-section showing core and build-up layers

Package thermal performance has been studied extensively for over a decade and a half. There have been several studies in the area of package and board level thermal performance. A representative sample is given in references (see [3]-[9]). Substrate design parameters that affect thermal performance of a flip-chip PBGA package are studied in [3]. It is concluded that substrate out-of-plane thermal conductivity and via placement is critical to realize good thermal performance. Calmidi and Sathe [4] studied the effect of packaging structure on the thermal performance of a

high-end flip chip BGA organic package. They concluded that even when no heat sink is used, by proper structural design, the thermal performance of an organic package can be made on-par with those that use high conductivity ceramic substrates. When a high performance heat sink is used in the application, substrate design is usually a very small effect. Board parameters that affect thermal performance at the system-level are discussed in [5]. Sathe and Sammakia [6] describe the thermal performance characteristics of a TBGA package. In addition to package thermal characteristics, detailed mathematical methods and practical considerations for such conducting such analyses are described. In [7], design considerations for thermal interface materials and heat spreaders for multi-chip modules are provided. Some of the concepts are applicable to single-chip packages as well. Shaukatullah et al. [8] studied die-attach thermal enhancement through the use of a radial finger contact (RFC) fitted between a flip-chip die and coverplate. Both, a dry contact and one using silicone gel are studied. More recently, Ramakrishna and Lee [9] studied the effects of underfill, thermal balls, heat spreader, and overmolding on the thermal performance of FC-PBGA packages. The substrate used in their study was 1.09mm thick and belongs to traditional "thick-core" technology. By contrast, the substrate in this study has a thickness of about 0.5mm.

This paper reports some of the thermal performance characteristics of flip-chip packages assembled with thin-core substrates under natural and forced convection conditions. An experimentally validated numerical model is used to conduct the study. The CoreEASEI substrate is used as a vehicle to perform the study. Specific focus is placed on the interaction between substrate and package assembly parameters on the thermal characteristics. It is noted that other system level parameters (board, flow bypass, heatsink, etc.) that can potentially affect thermal performance are not addressed in this study.

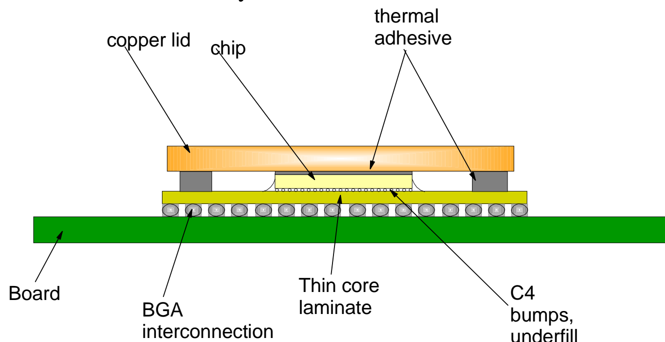

Figure 2: Cross-section of package assembly and test configuration used in this study

Package and Geometry Description

Figure 1 shows the cross-section of the substrate. It is a "2-4-2" cross-section with four metal layers in the core and two build-up layers above and below the core. The substrate is approximately 0.5mm thick, and core via pitch can be as low as 199μm. Core vias are 50μm in diameter. The dielectric material is a particle filled epoxy dielectric that is better suited for laser based processing in the core region than traditional thick-core substrates that employ glass cloth. An additional advantage of the particle filled epoxy dielectric is the higher thermal conductivity of 0.4 W/m-K. By contrast, epoxy resins are about 0.2-0.25 W/m-K. Figure 2 shows a schematic of a package assembly which contains an assembled package on a PCB that is used in this study. Figure 3 shows a plan view of the schematic of the model geometry. It shows the package on a PCB placed inside the test section of a wind tunnel. A package of size 42.5mm is attached to a board of size 101x105mm. The test board is built according to specifications in [14]. The chip size as shown is 14.7mm. There are two power planes of thickness 3.5e-2mm (1.4mils) in the PCB. The assembly is placed inside a cubical enclosure (wind tunnel) of size 0.3m. Four sides of the enclosure are solid walls. The remaining two sides are fluid inlet and outlet and are named as such (Figure 2). For cases where no air flow was simulated (i.e. natural convection), all six walls of the enclosure were considered to be solid.

Mathematical Formulation

Steady laminar flow and heat transfer is best described mathematically by the familiar Navier Stokes equations for momentum and energy given in Eqs. (1) in vector form [10]

$$\nabla.\rho u = 0 \tag{1a}$$

$$\frac{\partial \rho u}{\partial t} + (u.\nabla)\rho u = -\nabla p + \mu\nabla^2 u + \rho g \tag{1b}$$

$$\frac{\partial \rho C_p T}{\partial t} + (u.\nabla)\rho C_p T = \nabla^2 kT + S^r + Q''' \tag{1c}$$

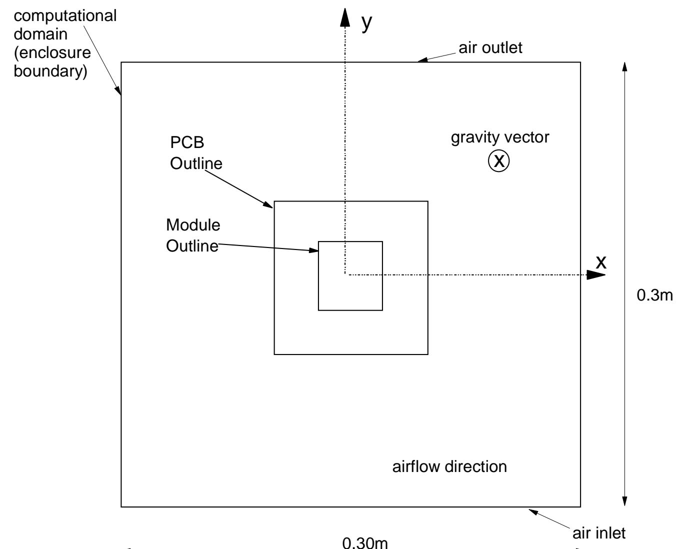

Figure 3: Plan view of the modeled geometry showing outline of enclosure, PCB, and package. Gravity vector is into the plane of the paper

The buoyancy force is accounted for using the ideal gas law (variable density). Variable viscosity and conductivity were assumed for the fluid (air) by fitting empirical data to a linear relation in the range of temperatures 0-300C [11]. As shown in Fig.3, the computational domain is coincident with the boundaries of the enclosure. The enclosure walls are located along the x=0.3m, z=0 m, and z=0.3 m planes. y=0 is

the inlet air opening and y=0.3 is the outlet air opening. x=0 is the symmetry plane. Also shown in Fig.3 are the gravity vector (into plane of the paper) and the airflow direction. The major (overall) dimensions are shown in Fig.3. Solid bodies are represented as blocks with appropriate thermal conductivity. Very thin layers (e.g. adhesive layers), where conduction is essentially one dimensional, are represented as effective thermal resistances. Air is assumed to be nonparticipating in the radiation calculations and all radiating surfaces (inner walls of the enclosure, top and bottom surfaces of the board) are assumed to be diffuse, gray with appropriate surface emissivities. The emissivity of the board surface (ε=0.8) and the copper lid (ε=0.25) is based on measured data reported in [12]. The enclosure walls are assumed to be black bodies. Surface-to-surface radiation is accounted by using a binary model. That is, all the radiative energy leaving surface 1, and arriving on surface 2 is accounted for. This includes direct transmissions from surface 1 to surface 2 as well as reflections of other radiating surfaces in the enclosure [11]

. When there are no reflections, the special case of radiative exchange between two bodies can be written as,

$$q_r'' = \sigma\left(\frac{1}{\frac{1}{F_{12}} + \frac{1-\varepsilon_1}{\varepsilon_1} + \frac{1-\varepsilon_2}{\varepsilon_2}\left(\frac{A_1}{A_2}\right)}\right)(<T_2>^4 - <T_1>^4)$$

where F12 is the geometric view-factor defined as the fraction of radiation leaving surface 1 which is intercepted by surface 2. The above equation represents the mode of radiation that is prevalent in this problem. The primary surfaces that radiate are the walls of the enclosure, the surfaces of the PCB and the module lid.

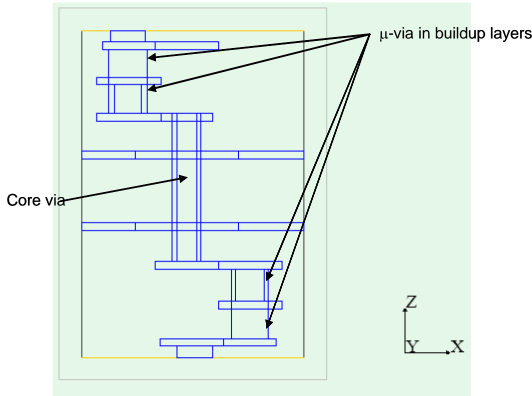

Figure 4: Cross-section view of C4 pad to BGA interconnection. Dielectric layers are not shown for clarity

Numerical Procedure

Modeling of high-density interconnections: A substrate with high-density interconnections can have several thousand copper connections from flip-chip pads to the ball grid array. These connections can dominate z-conduction (out of plane conduction) through the substrate and thus have to be accounted for accurately. Since it is not possible to include each one of these features in a numerical model, a "micro-macro" approach similar to [6] and [13] has been used in this study. A micromodel is used in a unit cell configuration to predict effective z-direction conductivity (k_{zz}) for the entire unit cell. This computed conductivity is then used as the effective conductivity of the substrate in the z-direction (see [13] for details). Since the region of the substrate under the chip has a high density of interconnections, two conductivities are used – one for the die region and one outside the die region. Figure 4 shows a cross-sectional view of the model of a typical signal connection within the substrate. The dielectric layers are not shown for clarity. In a typical application, it is unlikely that via density is uniform throughout. The recommended practice is to obtain an average via pitch by dividing the number of vias in the design by the total area under the die [13]. Figure 5 shows the variation k_{zz} as a function of average via pitch. As expected, k_{zz} decreases as via pitch increases since copper occupies a lower fraction of the unit cell cross-section. In this study, this micro-macro approach was used for the region under the die only due to high via density in that region. Outside the die-region, the effect of z-direction copper interconnections was neglected, due to very low via density.

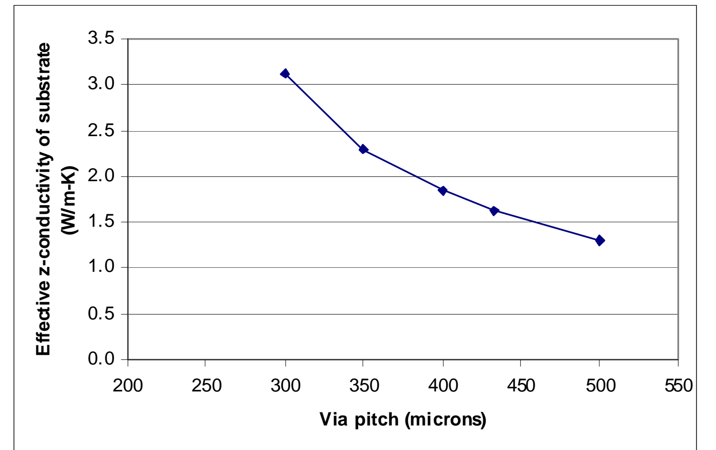

Figure 5: Effect of core via pitch on the effective out of plane conductivity (k_{zz}) of substrate

Material properties and thicknesses: Table 1 shows different layers in the substrate and board along with thicknesses and thermal conductivity values. Note that some layers are not used in all simulations since they are studied as a parameter (e.g. stiffener). The thickness values are considered to be nominal. The effect of thickness variation on thermal performance is not studied.

Table 1: Layer thicknesses and material properties

Layer	**Thickness (mm)**	**k(W/m-K)**	**Source**
Lid (copper)	1	380	[11]
Stiffener	0.61	18	[10]
Stiffener-Lid adhesive	0.18	1.4	Measurement
Stiffener-Laminate adhesive	0.13	0.2	Measurement
Silicon chip	0.74	Variable	[11]
chip-lid adhesive	0.09	1.0	Measurement
Underfill layer	0.1	0.6	Vendor
Laminate dielectric	Variable	0.4	Measurement
Board Cu planes (2X)	0.04	380	[10]
Board dielectric	Variable	0.3	Measurement

Boundary Conditions: The walls of the enclosure are exposed to still air. A uniform heat transfer coefficient of 5 W/mK is applied to the outer boundaries of the walls to simulate natural convection conditions. Changing this value between 2.5 - 7.5 W/m-K had virtually no effect on the chip junction temperatures. For the forced convection simulations, uniform air velocity is imposed at the air inlet and constant pressure at the air outlet. An ambient temperature of 20C and ambient pressure of 1.013×10^5 Pa are assumed. Computations were performed using the finite difference control-volume method in the commercially available software code Flotherm [11].

Grid Dependency: Variable grid spacing is used so that a finer spacing resulted in areas of relatively large gradients (typically close to solid boundaries). A grid dependency study was conducted by doubling the grid size in the regions of high gradients. Changing the grid size from 51X45X59 to 64X58X68 had little effect on the maximum temperature difference and velocity in the domain (0.4% and 6.5% respectively). Hence a grid size of 51X45X59 was used for all calculations. Convergence was assumed when the sum of residuals in the solution domain were less than 0.5% of the total heat generation for the energy equation and 0.5% of the characteristic flowrate for the momentum equations.

Experimental Validation: Prior to using the model for the parametric study, an experiment was performed to validate the model, geometry and material property assumptions. The test was performed with a package of size 42.5mm, chip size of 14.7mm, and board size of 101x105X1.56 mm per JEDEC standard JESD 51-9 [14]. In the test package a 1mm copper lid was assembled directly to the backside of the chip. The lid was coupled to substrate at the four corners using an adhesive pattern with a total effective area of $21mm^2$. The package assembled to the PCB was placed in a wind-tunnel as shown in the schematic in Fig.3. The thermal test chip was powered externally to 3W and the junction and air temperatures were monitored until steady state was reached (<0.1 C variation in 300 seconds), and then recorded. The test was repeated for various airflow rates. The experiment results are shown in Figure 6 along with the simulation predictions. The simulation predictions were obtained with k_{zz}=1.6W/m-K based on the average via pitch under the test die. A maximum difference (natural and forced convection) of 10.9% in θ_{ja} between model predictions and experiments was obtained.

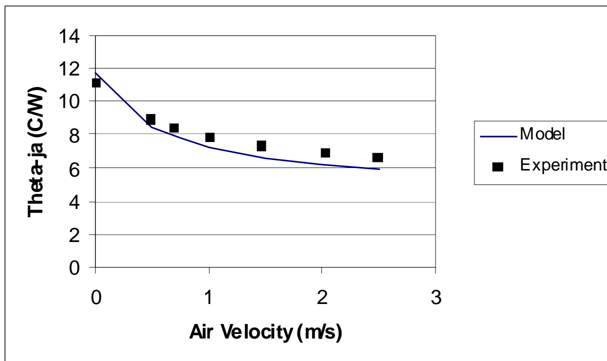

Figure 6: Comparison of Junction-to-ambient thermal resistance, θ_{ja}, between numerical results and experimental data. Power dissipation=3W

Results

The validated model described in the previous section was used to study the thermal performance of the package. For each case, a chip power of 3W and the desired air velocity was modeled. The quantities of interest are the chip temperature (reported as junction-to-ambient thermal resistance θ_{ja}) and major heat flows through the package. For all simulations, a body size of 42.5mm is assumed. The effect of the following parameters is studied:

1. die size (8mm and 14.7mm)
2. substrate out of plane conductivity (k_{zz} =0.6 and 3.1 W/m-K)
3. Lid assembly (see Figure 7):
   a. lid attached to back of die and corners to substrate (base case)
   b. lid attached to back of die and not coupled to substrate
   c. stiffener on substrate with lid coupled to stiffener

In each situation, specific focus is placed on how the parameters interact. Key to this is an understanding of the major heat flow paths within the package and the resultant impact on thermal performance. It is noted that substrate wiring design and lid assembly conditions listed above can affect overall package flatness. See [15] for a discussion of the relevant issues.

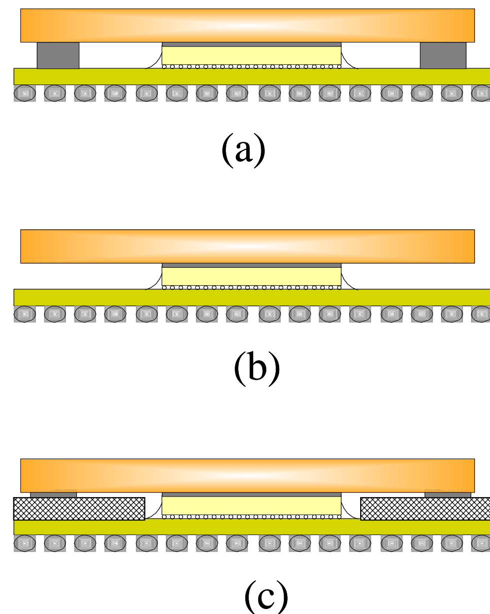

Figure 7: Three different package assembly conditions. (a) Lid coupled to substrate with "L" shaped dispense patterns at corners, (b) lid uncoupled from substrate, (c) Lid coupled to picture frame shaped metal stiffener around die

Base case: Figure 8 shows the junction-to-ambient thermal resistance θ_{ja} for the base case (i.e., package with lid attached to chip and coupled to corners of substrate as in Fig.7a). A chip power of 3W is assumed. As expected, θ_{ja} decreases with increase in air velocity for all cases. Shown in Fig.8 are

four curves combined into two sets. The first set refers to θ_{ja} with an 8mm die and the second refers to a 14.7mm die. In each set, the two curves refer to k_{zz}=0.6 and 3.1 W/m-K respectively. While increasing k_{zz} does decrease θ_{ja}, the difference is only about 6% and 5% for the 8mm and the 14.7mm die, respectively. This is in contrast with the results reported in [3] where a bigger difference was obtained by increasing the number of vias in the substrate. However, the study in [3] was for a package with a thicker substrate (1.096mm) and the package was lidless.

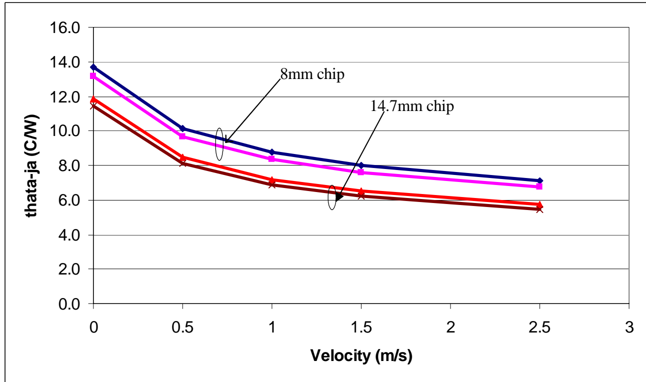

Figure 8: θ_{ja} as a function of air velocity for base case (lid coupled to substrate). Curves for k_{zz}=0.6 and 3.1 W/m-K are shown for each die size.

Additional insight can be gained by examining the heat flow paths within the package. Figure 9 shows the percentage of the total chip power from the bottom and top of the chip, and the bottom and top of the package respectively for k_{zz}=3.1 W/m-K. As air velocity increases, a greater fraction of the total heat leaves from the top of the die since the higher heat transfer coefficient lowers the lid-air thermal resistance. However, regardless of air velocity, note that the percentage of total heat leaving the top of the die is substantially greater than the percentage of the total heat leaving the top of the lid. For example, at 1m/s, 70% of the total heat leaves the top of the die whereas only 27% of the total heat leaves the top of the lid. The rest of the heat (43%) is bypassed through the lid-substrate attachment, substrate, and BGA into the PCB due to the lower thermal resistance offered by that path. Similar trends are obtained for the 14.7mm die as well with about 55% of the total heat leaving the top of the die at an air velocity of 1 m/s.

Lid not coupled to substrate: Figure 10 shows θ_{ja} as a function of air velocity for the case where the coupling between the lid and the substrate is removed (Fig. 7b). As in Fig. 8, the four curves are combined into two sets. Greater differences are observed by increasing k_{zz} from 0.6 W/m-K to 3.1 W/m-K when the lid is not coupled to the substrate. The enhancement is about 9% and 7% respectively for the 8mm and 14.7mm die respectively. Figure 11 shows the percentage heat flows from the top and bottom of the die and from the top and bottom of the package for a die size of 8mm and k_{zz}=3.1W/m-K. It is worthy to note that the heat leaving the top of the die is not the same as the heat leaving the top of the lid even when there is no coupling between the lid and the substrate.

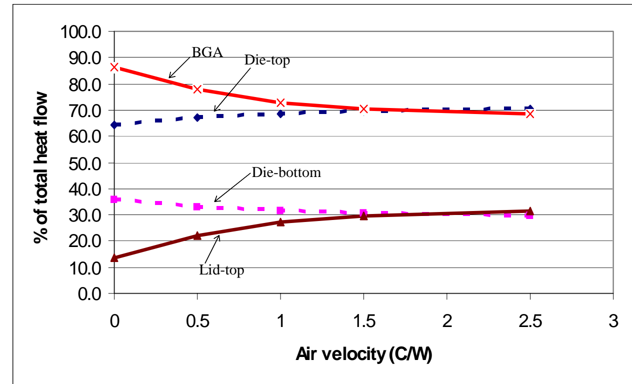

Figure 9: Die heat flow percentages from bottom and top of die and bottom and top of package. (k_{zz}=3.1 W/m-K, 8mm die, base case)

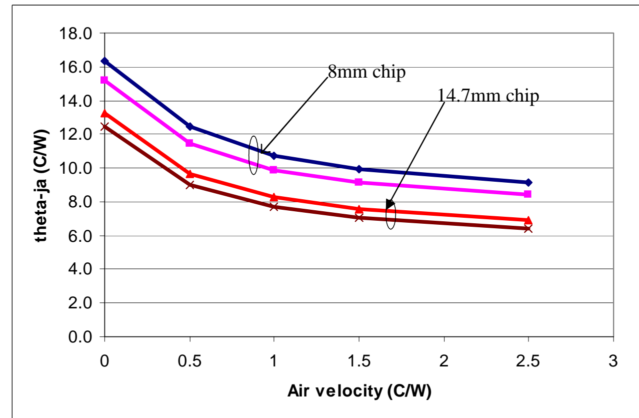

Figure 10: θ_{ja} as a function of air velocity when lid is not coupled to substrate. Curves for k_{zz}=0.6 and 3.1 W/m-K are shown for each die size

At first, this might seem unexpected. However, a careful examination of the thermal resistances involved clearly explain why this is the case. The area of the four corner contacts (Fig. 7a) is about 21mm^2, yielding a 1-D thermal resistance of about 23C/W. In comparison, the airgap between the bottom of the lid and the top of the substrate has a 1-D resistance of about 21 C/W with an 8mm die. Clearly, these two paths act in parallel, and when the lid-substrate coupling is removed, heat conduction in the air gap between the substrate and the lid also serves to enhance overall heat transfer albeit to a smaller extent. From Fig.11, at an air velocity of 1m/s, 57% of the total heat leaves the top of the die and about 34% leaves from the top of the lid. So, about 23% of the heat is diverted into the substrate through the air gap between the lid and the substrate. Recall that when there is physical coupling between the lid and the substrate (base case) about 43% of the heat is diverted from the lid into the substrate. Similar trends are observed for the 14.7mm die as well.

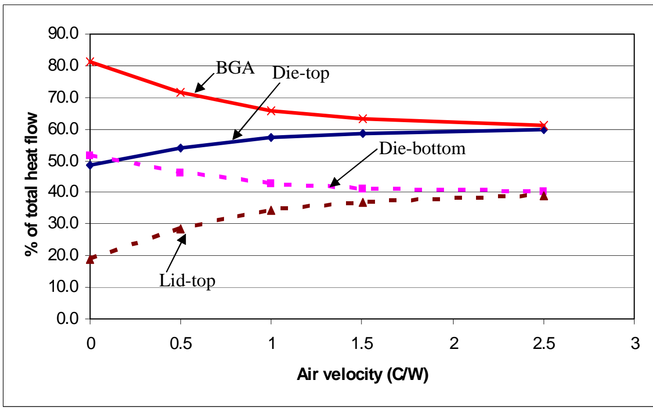

Figure 11: Die heat flow percentages from bottom and top of die and bottom and top of package. (k_{zz}=3.1 W/m-K, 8mm die, lid not coupled to substrate)

Thus, as an extension, it can be expected that when no lid is used on top of the flip-chip die, the enhancement from adding additional core vias is the most among the cases studied here. Since no lid was assumed in the study in [3], a large improvement in thermal performance was observed due to addition of core vias.

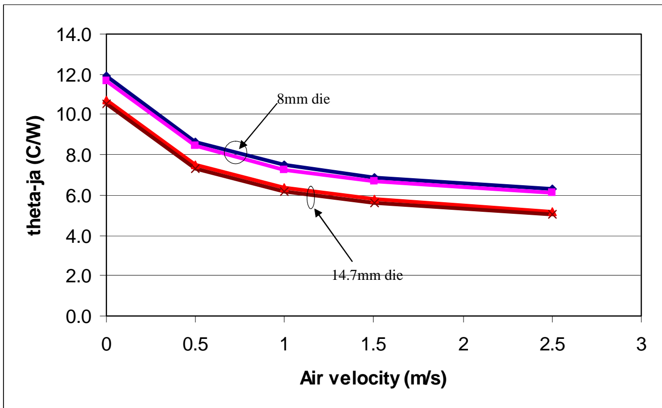

Figure 12: θ_{ja} as a function of air velocity when lid is coupled to stiffener on substrate. Curves for k_{zz}=0.6 and 3.1 W/m-K are shown for each die size

Stiffener on substrate with lid coupled to stiffener: A stiffener is sometimes used to improve flatness of the substrate to aid in chip assembly and board assembly operations [15]. It is the same size as the substrate with a punched hole to accommodate the die. Typically, the hole is sized about 6mm larger than the die. A schematic of this configuration is shown in Fig. 7a. The stiffener plays the dual role of reducing the thickness occupied by the lid-substrate coupling material (as well as the air gap), and additional heat spreading in the substrate. Thus, from the heat conduction mechanisms presented so far, it can be expected that the presence of a stiffener will improve thermal performance by reducing the thermal resistance of the heat path from the lid to the substrate. Figure 12 shows the θ_{ja} as a function of air velocity for the package configuration in Fig. 7c. The additional thermal enhancement by changing k_{zz} from 0.6W/m-K to 3.1W/m-K is minimal (about 3%) for both 8mm and the 14.7mm die sizes.

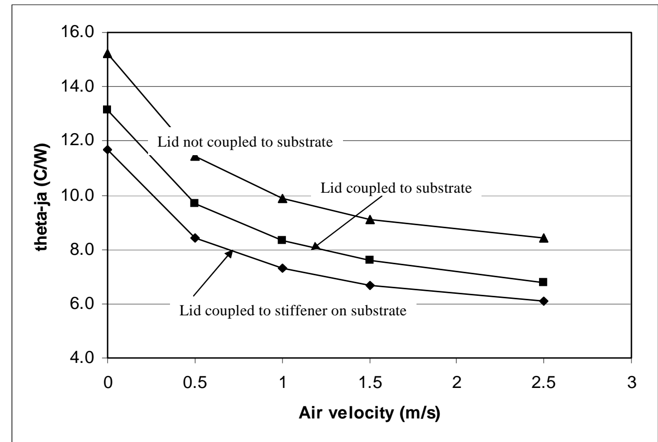

Figure 13: θ_{ja} as a function of air velocity for three different lid assembly conditions. (k_{zz}=3.1 W/m-K, 8mm die)

Figure 13 shows a comparison of the θ_{ja} for the three lid assembly conditions in Fig.7. A k_{zz} value of 3.1 W/m-K has been assumed. The thermal resistance for the base case (Fig 7a) is about 10-15% higher than when a stiffener is used in the package. When the lid is not coupled to the substrate (Fig. 7b), the thermal resistance is 30-38% higher than when a stiffener is used. Clearly, when a stiffener is used in the package a substantial improvement in thermal performance is obtained. This finding is similar to the one reported in [12] which showed minimal changes in thermal resistance when the laminate dielectric conductivity was changed from 0.5 to 20 W/m-K, when a stiffener was used in the flip-chip package.

Summary and Conclusions

The thermal performance of a thin, high interconnect density substrate for flip-chip applications, CoreEASEI ™ has been studied. The package is assumed to be assembled to a PCB per JEDEC standard conditions [14]. The parameters that were varied are:

a) die size (8mm and 14.7mm)

b) effective via pitch (substrate out of plane conductivity k_{zz})

c) lid assembly conditions (see Figs. 7 a,b,c)

Chip temperature and heat transfer within the package are primary quantities of interest. The major conclusions of the study are as follows:

1. The effect of increasing the number of vias was studied by varying k_{zz}, the substrate out of plane conductivity. It was found that the effect of increasing k_{zz} was different for different lid assembly conditions. When no lid-substrate coupling is present (Fig. 7b), an enhancement of up to 9% was obtained. When lid coupling was present (Fig.7a), the enhancement was up to 6%. When a stiffener was present, the enhancement was almost negligible at 3%.
2. When a stiffener is used in the package (Fig 7c), the enhancement is about 10-15% over a coupled lid package (Fig 7a), and 30-38% over lid uncoupled package (Fig 7b). This enhancement is due to a primary heat flow path from the lid, to the stiffener, through the substrate into

the BGA. The implication is that the thermal performance of the substrate can be improved without resorting to thermal vias, etc., thus reducing substrate manufacturing costs, and improving wiring flexibility.

3. When no stiffener is present in the substrate, physically coupling the lid to the substrate (Fig 7a), improves thermal performance by about 13-20%. This can further be improved by increasing the contact area of the lid-substrate coupling material and optimizing the dispense pattern.
4. When no lid-substrate coupling is present (Fig 7b), even the air gap between the lid and substrate plays a role in transferring about 50% of the heat flowing from the die to the lid into the substrate. This has implications in high altitude and space applications where air density is substantially low or vacuum conditions are prevalent. Under these conditions, the lid-substrate thermal coupling is compromised.
5. The theta-ja values for the smaller die size are larger, as expected. However, the relative effect of the parameters studied (k_{zz}, lid assembly conditions) on the theta-ja for the two die sizes are similar (within a few percent).
6. The theta-ja values obtained are for one set of board conditions [14] and system conditions (i.e. no heat sink). Changing board conditions might affect theta-ja values. However, trends reported in this paper are not expected to change.

Acknowledgments

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