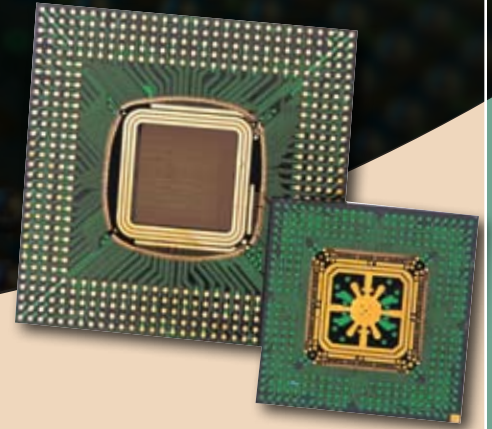
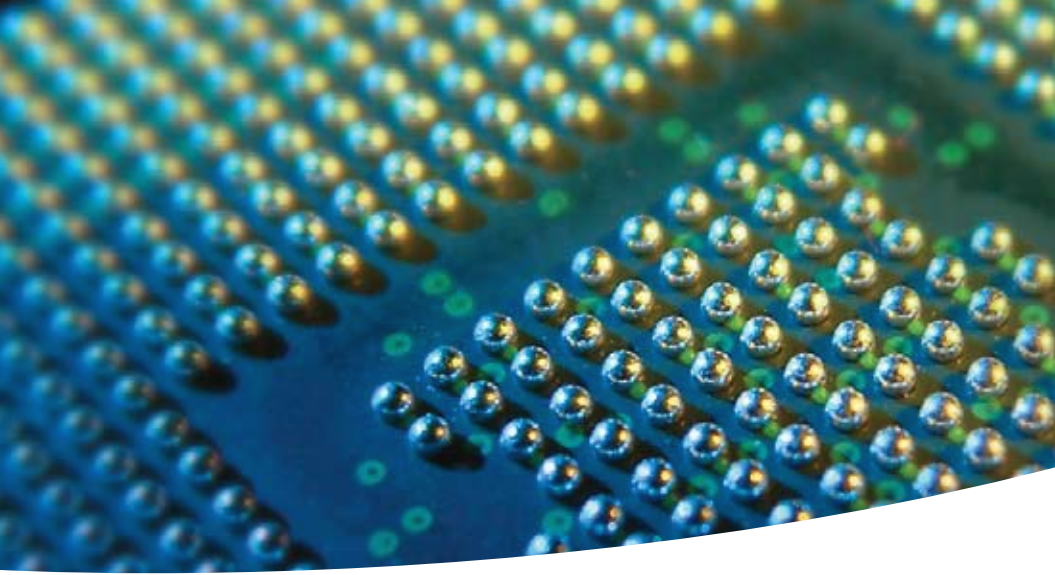


Wire Bond PBGA



High performance packaging for wire bond die

El's organic wire bond plastic ball grid array (PBGA) carriers provide leading edge, system-in-package (SiP) or single-chip module (SCM) precision packaging solutions for semiconductor technology. Superior electrical performance, combined with materials that are matched to the printed circuit board, allow wire bond PBGA carriers to deliver high overall performance and field reliability.

If you're looking to extend the use of your existing wire bond infrastructure, these PBGA carriers are available in both chip-up and cavity configurations. The chip-up design is extremely economical and targets lower power applications while the cavity package allows the backside of a die to be thermally connected to a heat spreader. This configuration is mounted to a printed circuit board with the heat spreader exposed, allowing easy attachment of a heat sink and providing excellent thermal performance.

Features

Pick and place compatible

Standard JEDEC body sizes and testing

Single tier cavity

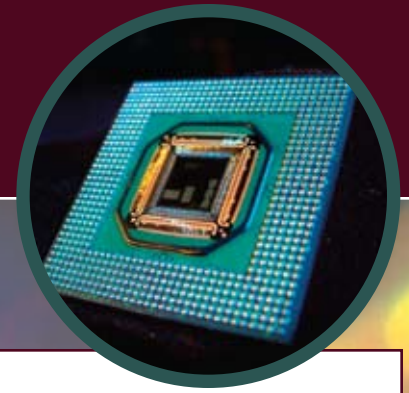
Single layer or multi layer cross sections

Support for standard chip-up or cavity
for added thermal performance

Available in BT, Polyimide or FR4
dielectric materials

the power of performance

Wire Bond PBGA technology



Unleashing the Power of Silicon

El's wire bond PBGA packages help you realize the potential of your silicon. Wire bond PBGA is produced using dense circuitization processes on high volume circuit board equipment.

Features

Bondfinger pitches of 118 μ m enable shorter wire lengths, die shrinkage or higher I/O density

Allows a reduced distance between the edge of the die and the bondfinger

Ability to support more voltage and ground connections

Shorter wire bond wires, lower loop heights, and increased V/G connections result in significantly reduced electrical parasitics of an assembled module

Provides the ability to migrate from a chip-up package to a same size cavity package as chip power requires

Single part number substrates can accommodate a greater chip part number mix, providing increased I/O capability

Specifications

Performance

Die interconnect	Wire bond, 60 μ m inline, 43 μ m staggered
Card interconnect	BGA available down to 1.0mm full grid array
Package I/O count	Greater than 700
Standard compliance	JEDEC Class 3
Body size	JEDEC standard

Materials

Conductor	Copper
Dielectric	BT, polyimide, FR4

Mechanical Properties

Substrate thickness	1.0mm
Typical PTH diameter	0.25mm
Bond finger pitch	118 μ m, no lines between pads 194 μ m, one line between pads (97 μ m effective pitch)
BGA	1.0mm, 1.27mm

Typical Electrical Characteristics

Impedance Zo	60-100 Ohms (with ground plane) 120-150 Ohms (no power planes)
Line resistance	1.0-1.5 Ohms/cm
Propagation delay	65-70 ps/cm

For more detailed information about our wire bond PBGA technology, call us today at 866-820-4820. Our application engineers are ready to assist you with detailed information for successful product usage. You can also visit our website at www.endicottinterconnect.com.



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For more information, visit our website at www.endicottinterconnect.com