Wireability Comparison of Flip Chip Substrates as a Function of Chip Design and Substrate Capability

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Abstract

As flip chip grows in usage it becomes increasingly important to determine the wiring capability of flip chip substrates as a function of chip design and substrate capability. This paper defines a flip chip standardized footprint that allows comparisons to be made for the key variables. The footprint has a mix of signal and power I/Os with the signal escape that can best be classified as peripheral. It then explores the major variables that the designer has available including flip chip bump pitch, chip size, substrate layer count, substrate build-up layer density, substrate core layer density plus substrate via and plated through hole capability. The end result is a set of graphs that show wiring capability vs. chip size for the variables that have been examined. These graphs can be used by the designer to determine the chip size and substrate capability required to execute the design in the most efficient manner. The substrates used in this study are of the build-up variety and a key variable that is explored is the density of the core plated through holes. Chip bump pitch is explored from 150 um thru 225 um and chip size from 6 mm through 18 mm. Substrate build-up layers of one through six are included. In all cases, the signal lines maintain nearby reference planes for good electrical performance. The paper will also go through the substrate design steps layer by layer with an objective to provide maximum wiring capability using the available design parameters. The results of this study can help the designer achieve the most cost effective combination of chip design and substrate selection while maintaining good electrical performance. This allows effective co-design of the chip and substrate which can significantly reduce the cycle time for new products.

Key Words: Chip, substrate, flip chip, design, wiring, escape, core, PTH pitch

Introduction

The increasing demand for more function and higher speed has accelerated the introduction of flip chip to provide the required number of signals and meet electrical performance requirements. Flip Chip footprints have been developed in a variety of ways starting with a peripheral approach that mimics the footprint of a wire bonded chip. This approach salvages the basic chip design and allows conversion from wire bond to flip chip. IBM originally introduced flip chip technology and nicknamed the I/O as C4. A typical conversion from wire bond to flip chip is illustrated in figure 1 which show a corner area of each chip type. The approach shown in figure 1 does not take full advantage of flip chip technology and has signal escape capability that is similar to wire bond escape capability. Therefore, it is desirable to extend the signal I/O capability further from the chip edge towards the center of the chip. This allows more signals to be placed on the same sized chip or allows a reduction in chip size for the same number of signals. Chips that can take advantage of this approach are said to be "I/O bound" and the "I/O bound" situations have increased significantly as chip feature size is reduced thereby decreasing chip area requirement for the same amount of function. "I/O bound" situations occur more often in ASIC chip designs where the multiple functions inside the chip drive additional I/Os. We will define I/O density as the ratio of chip signal I/O to chip area. A chip with 8 um chip feature capability might use only 38% of the area for the same functional capability as a chip of 13 um chip feature capability assuming that the area needed is a function of the square of feature size. If the same number of chip I/O is still required, the 8 um chip requires much higher I/O density to take full advantage of the decreased chip feature size. In actual cases the newer chip technologies are accompanied by a demand for more function than the technology it replaces, thereby needing more area for the functions and raising the 38% ratio somewhat but still requiring a much smaller chip. In almost all cases the newer chips will have a higher I/O density than the chips they replace. Fortunately, substrate technology has been improving steadily and can meet higher I/O requirements but sometimes at an excessive cost which reduces the economic savings achieved with smaller chips. This study looks at substrate feature sizes and capabilities to determine the commonly available combinations that can satisfy chip I/O demand. The study is based upon organic based substrates with build up layers similar to the Surface Laminar Circuit^{TM} [1] technology introduced by IBM Yasu in the early 1990s. Important elements in this study are the number of substrate layers and the hole density of the central core of the substrate. It will be shown that as the core hole density increases, the general usefulness of the substrate layers increases dramatically [2]. Another variable that is very important is chip size and it will be shown that smaller chips do not require as high a substrate complexity as larger chips.

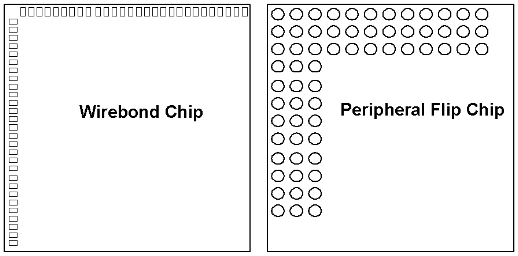

Figure 1 - Wire Bond Chip Footprint vs. Peripheral Flip Chip Footprint

Chip Footprint Definition

The definition of a chip footprint for this study required a universal approach that would have the potential for good electrical performance and could permit the chip C4 to be as deep as possible, only limited by chip size and substrate capability. The approach that seemed to satisfy this was to use alternating columns of signal C4s and power/ground C4s. It is fairly common to place alternating columns on an interstitial pitch to give the highest chip I/O density with a maximum pitch between C4s. These key elements produced the basic design noted in figure 2 with the basic distance between C4 designated as the chip pitch and the interstitial distance as half of the chip pitch. The pattern shown in figure 2 is not limited to the number of I/Os shown in figure 2 but can continue away from the chip edge until the chip area is fully consumed or the substrate wiring capacity is fully consumed and deeper signals are not justified.

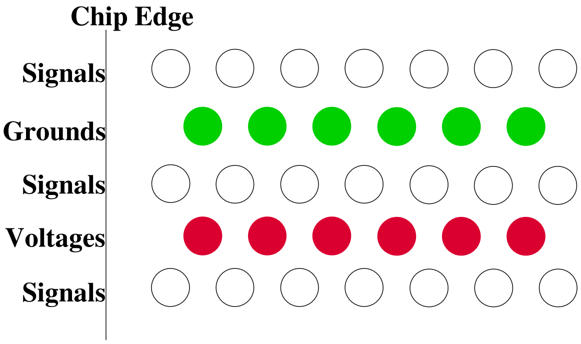

Figure 2 - Reference Chip Footprint

Another key element of the chip footprint is the construction of the footprint in the corner of the chip. This is shown in figure 3 and for the purpose of succeeding calculations, the distance from the chip edge to the center line of the first C4 row is set at 200 um. The open circles are signals just as in figure 2.

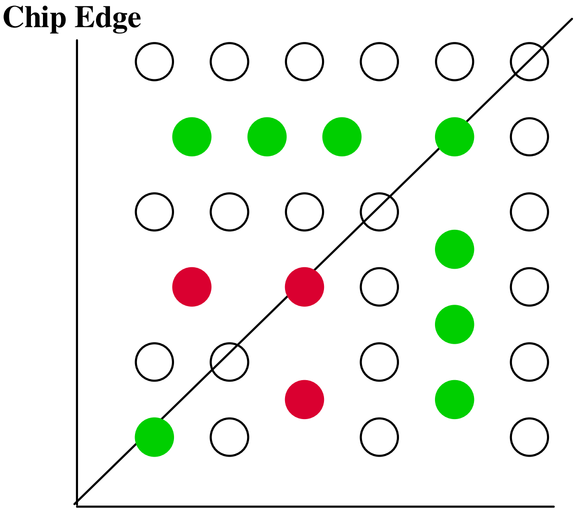

Figure 3 - Chip Corner Footprint

Using the chip corner as a starting point and the reference chip footprint noted above, the relationship between depth of signals and chip size can be established. If the basic chip pitch is 200 um, the corner element shown in figure 3 will use 1200 um from the chip edge to the center line of the third set of signals. If the third set of signals was at the center of the chip, the chip size would be 2.4 mm and the signal depth would be 6 deep. Table 1 shows signal depths for various chip sizes with various chip pitches using the chip footprints of figures 2 and 3.

Table 1 - Signal Depth vs. Chip Size and Chip C4 Pitch

Chip Size (mm)	Signal Depth		
	175 um C4 Pitch	200 um C4 Pitch	225 um C4 Pitch
6	16	14	12
10	27	24	20
14	38	34	28
18	50	44	36

The signal depths shown in table 1 are rarely achieved but they represent the maximum possible with the available chip area using the footprint definition of figure 2 and figure 3. Therefore, the limitation on signal depth will become the wiring capacity of the substrate that mounts the chip. With these footprints, substrate density features can be fully utilized to increase signal depth and get the maximum number of signal I/Os for a given chip size. In order to simplify the exploration of substrate variables, a C4 pitch of 200 um will be used for all the substrate explorations but the conclusions can be applied to any C4 pitch.

Substrate Design Approach and Variables

The basic substrate type that will be used for this study is a build up substrate with a central core layer and one or more build up layers on either side of the core. The top layer is the C4 layer that will mate with the chip. The bottom layer has an array of pads that will have an array of balls attached (BGA) and this BGA layer will mate with the printed circuit card. The central core usually has either two or four layers. For this example, the two layer core will have power layers on each side and the four layer core will have embedded power layers and signal layers on the surface of the core.

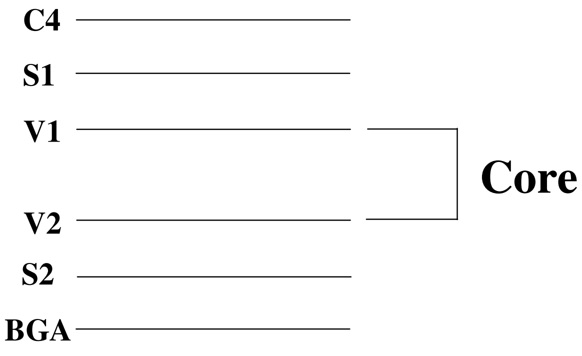

Figure 4 - Cross Section of 2-2-2 Substrate

A six layer substrate with two signal layers can be constructed either way with the two layer core designated as a 2-2-2 and shown in figure 4 and the four layer core designated as a 1-4-1 and shown in figure 5.

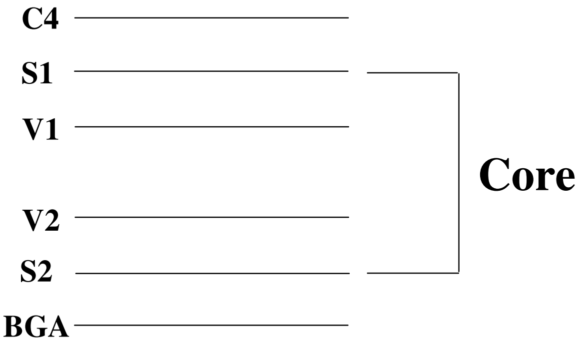

Figure 5 - Cross Section of 1-4-1 Substrate

Additional build up layers can be added to either substrate to increase the number of signal layers thereby providing additional wiring capability and deeper signal escape. For example, two additional layers on a 2-2-2 substrate would make it a 4-2-4 and the number of signal layers would increase from two to four. Similarly, two layers added to a 1-4-1 substrate would result in a 3-4-3 with four signal layers.

Now that the basic substrate cross section is defined, the design approach can be addressed. One of the keys to achieving maximum wiring capability is to free the signal planes of obstructions as much as possible so that the signal plane wiring capacity can approach the capability defined by the line width and line spacing minimums. As an example, if the minimum line width is 25 um and the minimum line space is 25 um a line can be placed at 50 um centers and the wiring capacity would be 20 lines per mm. However, if the channel for line spacing had a 90 um diameter via pad every 200 um, only 110 um would be left for wiring. Since we need 25 um space between the via pad and the first line, only one line could be wired between these vias. This translates to one line per 200 um centers or 5 lines per mm which is well below the line / space capability of 20 lines per mm. The first area that can help create additional signal channel spacing is by commoning the power and ground pads on the C4 layer. The depth of commoning should be great enough to create a channel that can be filled to full capacity with signals on the S1 layer. Using the 200 um C4 pitch example, commoning the power and ground pads will create a 400 um channel on S1 which is reduced by 90 um for the outermost signal pad and reduced by 25 um spacing from the pad to the first line. This leaves 285 um for wiring which equates to 5 lines per channel using 25 um lines and spaces. Therefore, the power and ground commoning on the C4 layer only needs to be two or three deep which will have minimum impact on power distribution. The escape on S1 can be further improved by repositioning the outer signal on the C4 layer so that it is not part of the channel restriction. The net result is to escape 7 signals on S1 for every 400 um pitch which results in a wiring capacity of 17.5 signals per mm, a major improvement over 5 lines per mm with via blockages every 200 um. This is very close to the maximum of 20 signals per mm with 25 um lines and spaces. By selectively applying commoning and signal redistribution the S2 layer can have an 800 um channel with a single via blockage. With 675 um available for signal wiring 13 lines per channel are possible and 14 lines can be escaped for every 800 um pitch on S2 thereby achieving an S2 wiring capacity of 17.5 lines per mm. Figure 6 shows the C4 layer of this design strategy and figure 7 shows the S1 layer. The color coding of figure 2 is maintained and the small circles within the pads represent microvias which will communicate to the layer below. The segment shown repeats along the entire edge until the corner area where the wiring is less dense because the signal depth is lower in the corners.

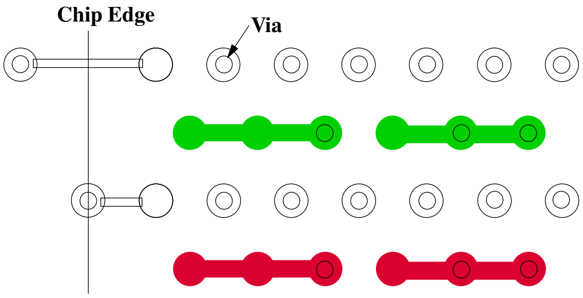

Figure 6 - C4 Layer Wiring

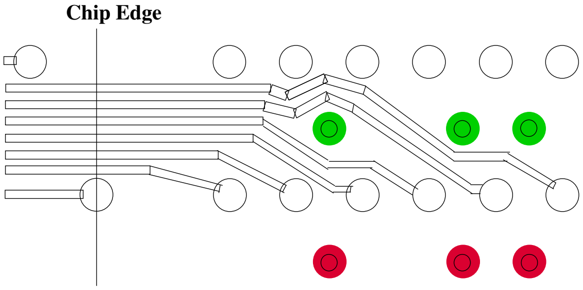

Figure 7 - S1 Layer Wiring

The next step in the wiring strategy is to determine how many signals can be routed through the core to the lower half of the substrate cross section. If the core is mechanically drilled, the pitch between holes in the core layer is normally greater than 500 um and there is no room in the area under the chip to route signals. The core vias would be reserved for power distribution. With the introduction of thin cores drilled with laser vias or very small mechanically drilled vias, the possibility of routing signals to the lower half of the substrate becomes practical. A good objective is to have a core via pitch that can provide enough signals to supply the wiring density capability of the S2 layer and still have vias left over for power distribution. Any substrate that meets these requirements will be referred to as a “Dense Core” substrate to differentiate it from substrates with normal core via pitches. Table 2 shows the core via pitch required to meet “Dense Core” definition. It is shown as a function of C4 pitch using 25 um lines and spaces and a 90 um diameter via pad.

Table 2 - Dense Core Via Pitch

C4 Pitch (um)	“Dense Core" Via Pitch (um)
175	208
200	237
225	267

With the chip footprint and design strategy established, the impact of substrate variables on wiring capability can be explored. The key variables that are examined are the following:

- Line width and space capability
    - 20 um lines and spaces
    - 25 um lines and spaces
    - 30 um lines and spaces
- “Dense Core” vs. Standard Core
- Signal layers – 2 and 4
- Chip Size
    - 6 mm
    - 10 mm
    - 14 mm
    - 18 mm

The study will assume a C4 pitch of 200 um and assume a via pad size of 90 um but the conclusions will apply to a fairly broad range of C4 pitches. The standard core design will require a 4-2-4 or 3-4-3 cross section (10 layers) to achieve 2 signal layers because there is no wiring in the bottom half of the cross section. It will require a 8-2-8 or 7-4-7 cross section (18 layers) for 4 signal layers. “Dense Core” requires 2-2-2 or 1-4-1 (6 layers) to achieve 2 signal layers and 4-2-4 or 3-4-3 (10 layers) to achieve 4 signal layers. For simplification final results will be shown as total layers instead of a specific cross section. A 14 layer with 3 signals will also be shown for standard core.

Wiring Capability

The wiring capability will be divided into two sections. The first section defines peak wiring capability which would be applied to the center of the chip edge and is independent of chip size. Next, actual wiring capability for a given chip size which accounts for the reduced number of C4s in the corners of a chip. The approach will assume that the C4 layer can redistribute pads so that the S1 layer has one pad for each 400 um of wiring channel width. Also, an additional signal is redistributed on the C4 layer to add to the total wiring on the S1 layer per figures 6 and 7. Additional redistribution allows S2 through S4 to have only one pad for each 800 um of wiring channel width. Table 3 shows the design elements examined and the wiring capability of the various layers using those assumptions.

Table 3 - Wiring for Each Layer vs. Line Width and Space with 200 um C4 Pitch and 90 um Pad

Line Width (um)	Line Space (um)	S1 Wiring (signals/mm)	S2 thru S4 Wiring (signals / mm)
20	20	17.5	22.5
25	25	17.5	17.5
30	30	15.0	15.0

In this specific example the extra pad blockage on S1 reduced the effectiveness of the potentially denser 20 um lines and spaces vs. 25 um lines and spaces. However, as the pad blockage decreased on the S2 thru S4 layers, the wiring capability is a direct function of the line width and space density. Total wiring depends upon the number of signal layers in the cross section. Table 4 shows the cumulative wiring vs. line width and space for both two signal layers and four signal layers.

Table 4 - Wiring for 2 and 4 Signal Layers vs. Line Width and Space with 200 um C4 Pitch and 90 um Pad

Line Width (um)	Line Space (um)	2 Signal Layer Wiring (signals/ mm)	4 Signal Layer Wiring (signals/mm)
20	20	40	85
25	25	35	70
30	30	30	60

The cross section to achieve two or four signal layers will depend upon the core via density and is differentiated by standard core and "Dense Core". Since cost of the substrate is dependent on total layers plus layer density it is useful to examine the plot of wiring capacity vs. total layers as shown in figure 8. The largest effect is "Dense Core" vs. standard core which is most easily seen by examining the wiring signal escapes per mm at 10 layers.

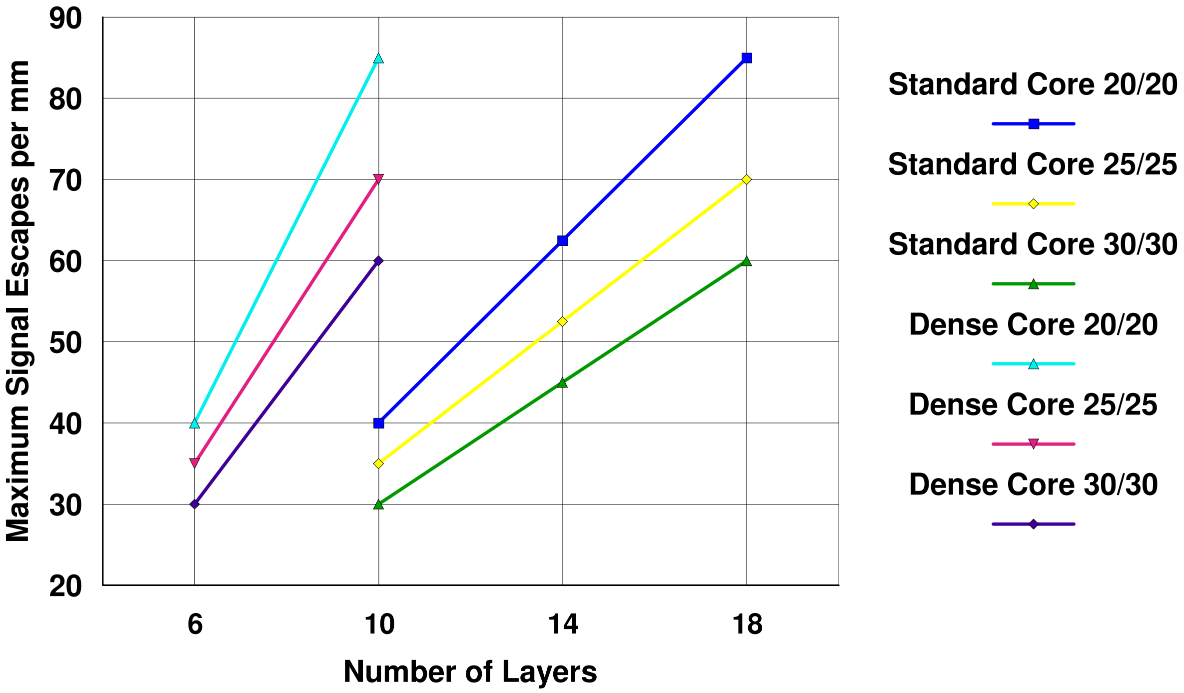

Figure 8 - Signal Escapes vs. Number of Layers – 200 um C4 Pitch

Next most important variable is line width and space capability but increasing wiring capacity through feature size reduction might be accompanied by increased cost. In many cases capability to produce these finer features may not exist or could result in greater percentage variations in line width which would lead to poorer electrical performance. In figure 9, the wiring capability is normalized by dividing wiring capability by total number of layers in the substrate. Examining figure 9, the "Dense Core" population is positioned to provide significantly higher wireability per layer because of the utilization of the lower half of the substrate for wiring. As an example, a six layer "Dense Core" substrate with 25 um lines and spaces has more signal escapes per layer compared to an 18 layer standard core with 20 um lines and space.

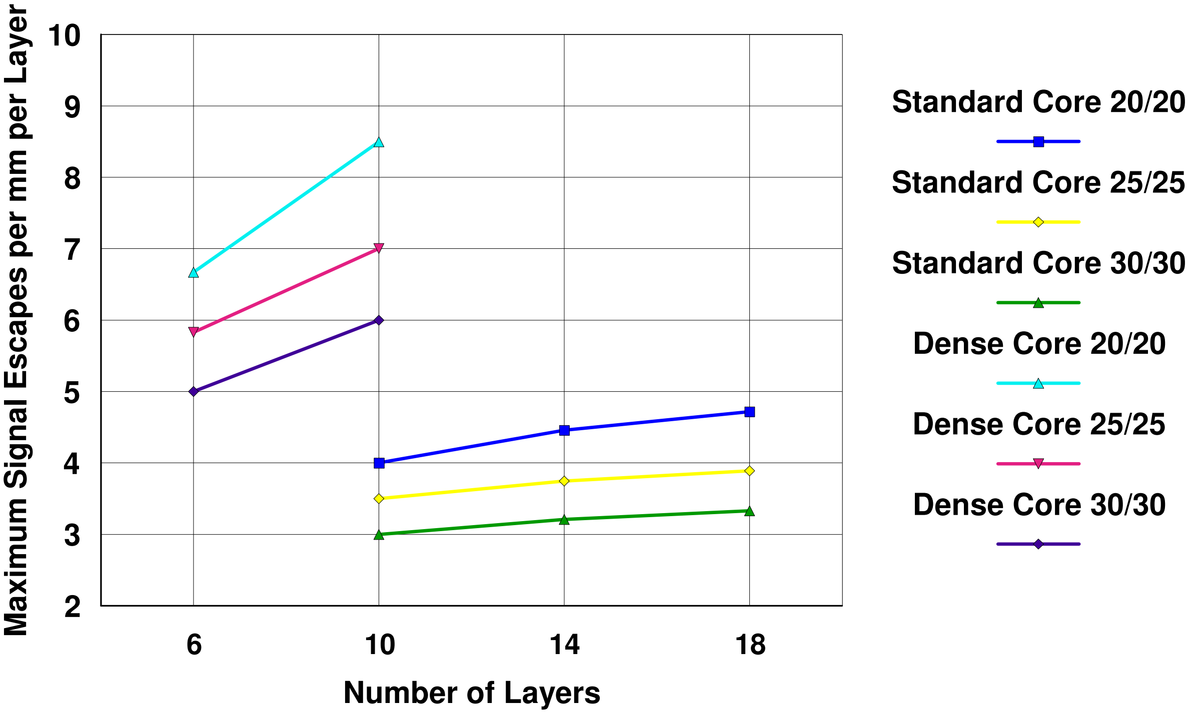

Figure 9 – Signal Escapes per Layer vs. Number of Layers - 200 um C4 Pitch

Effect of Chip Size

Figures 8 and 9 apply to the area of the chip that is beyond the corners and therefore is referred to as maximum signal escapes. For actual chips the corner must be considered and as will be seen this is most significant for smaller chips. Table 1 shows the attainable signal depth as a function of chip size. This signal depth is applied against the available wiring choices to determine whether full signal depth is achievable. Once full signal depth is achieved there is no value in increasing the number of layers or striving for finer features. As an example, table 4 indicates that two signal layers with 30 um lines and spaces can provide 30 signal escapes per mm on a chip with a 200 um C4 pitch. This equates to 12 deep because the signal pitch per figure 2 is twice the C4 pitch or 400 um and 30 signals per mm multiplied by 0.4 mm signal pitch equates to 12 deep. This is nearly enough to satisfy the full depth of a 6 mm chip which is 14 deep per table 1. The maximum chip depth for 200 um C4 pitch and the substrate limited depth vs. feature size for both two and four signal layers is noted in table 5. The substrate signal data is truncated to be no higher than the chip maximum signal depth. For a 6 mm chip, two signal layers with 25 um lines and spaces achieves full signal depth and added signal layers or finer lines and spaces are not necessary. For a 10 mm chip, full depth is achieved with four signal layers using 30 um lines and spaces. A 14 mm chip requires four signal layers with 20 um lines and spaces to achieve full depth and for the 18 mm chip, full depth is not achieved for any of the substrate design points shown in table 5. The information in table 5 can be translated into signals per mm for various chip sizes.

Table 5 - Maximum Signal Depth vs. Chip Size and Substrate Properties - 200 um C4 Pitch

Chip Size (mm)	Chip Max. Signal Depth	Line Width (um)	Line Space (um)	2 Signal Layer Max. Signal Depth	4 Signal Layer Max. Signal Depth
6	14	20	20	14	14
		25	25	14	14
		30	30	12	14
10	24	20	20	16	24
		25	25	14	24
		30	30	12	24
14	34	20	20	16	34
		25	25	14	28
		30	30	12	24
18	44	20	20	16	34
		25	25	14	28
		30	30	12	24

The following four figures show actual signal escapes for each of the chip sizes noted in table 5. These figures will become the basis for the interaction between chip demand and substrate capability. Use of these figures will be illustrated to show how substrate designs can be rapidly selected. A 6 mm chip truncated at 12 deep has signal depths of 1, 3, 5, 7, 9, 11 and 12 as it works its way from the corner of the chip to the center of the chip. There are also some additional signals on the chip diagonal. Figure 3 is a guide to show the increased signals as one moves from the corner of the chip to the center. Total escapes for a 6 mm chip truncated at 12 would be 408 signals. If the full depth of 14 was attainable, the sequence would be 1, 3, 5, 7, 9, 11, 13 plus an additional signal on the diagonal. This equates to 420 signals which is only a small improvement over 408 signals attained at 12 deep. Figures 10 through 13 show the actual signal escape as a function of layer count and substrate design. Figure 10 shows that a fairly low density 6 layer substrate with 2 signal layers is adequate for a 6mm chip.

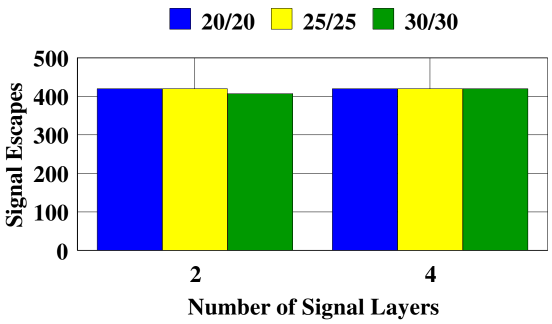

Figure 10 - Signal Escapes for 6 mm Chip vs. Signal Layers and Substrate Density - 200 um C4 Pitch

Figure 11 is a similar plot for a 10 mm chip and the sequence does not become truncated for any of the two signal layer substrates but gets truncated for all of the four signal layer substrates which indicates that 30 um lines and spaces will do as well as 20 um lines and spaces for this chip size. The sequence for the 10 mm chip is 1, 3, 5, 7, 9, 11, 13, 14, 14, 14, 14 and 14 and some additional signals on the diagonal for the two signal layer designs at feature sizes of 20 um or 25 um. Many of the chip available signals are not escaped with two signal layers. For four signal layers, the sequence is 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21 and 23 with additional signals on the diagonal. The net result is plotted in figure 11 which shows an advantage for four signal layers but not as large an advantage as the base wiring capability would suggest.

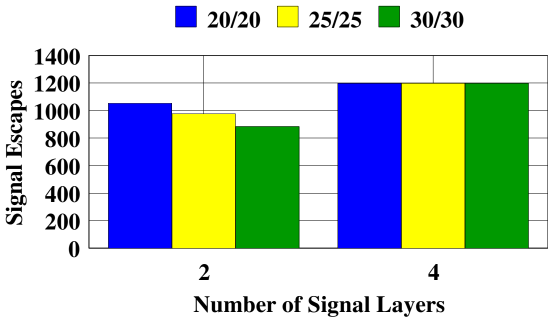

Figure 11 - Signal Escapes for 10 mm Chip vs. Signal Layers and Substrate Density - 200 um C4 Pitch

As chip size increases further, even four signal layer substrates will be truncated by substrate limitations and the advantage of four layers vs. two layers increases. This is illustrated in figures 12 and 13 which show the results for 14 mm and 18 mm chips respectively.

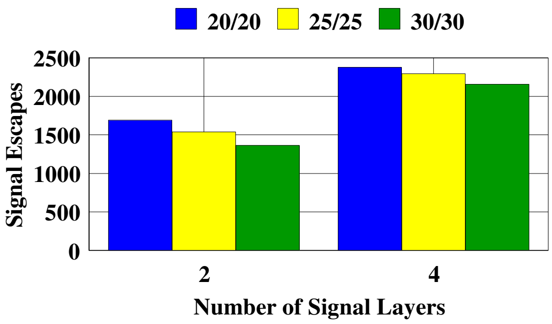

Figure 12 - Signal Escapes for 14 mm Chip vs. Signal Layers and Substrate Density - 200 um C4 Pitch

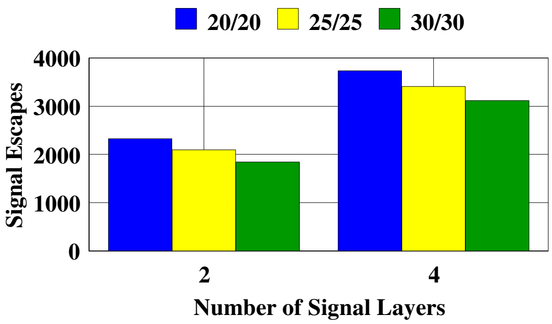

Figure 13 - Signal Escapes for 18 mm Chip vs. Signal Layers and Substrate Density - 200 um C4 Pitch

Figures 12 and 13 can be integrated to give a line graph that allows estimates for any chip size vs. the six combinations of signal layers and layer density. This is shown in figure 14.

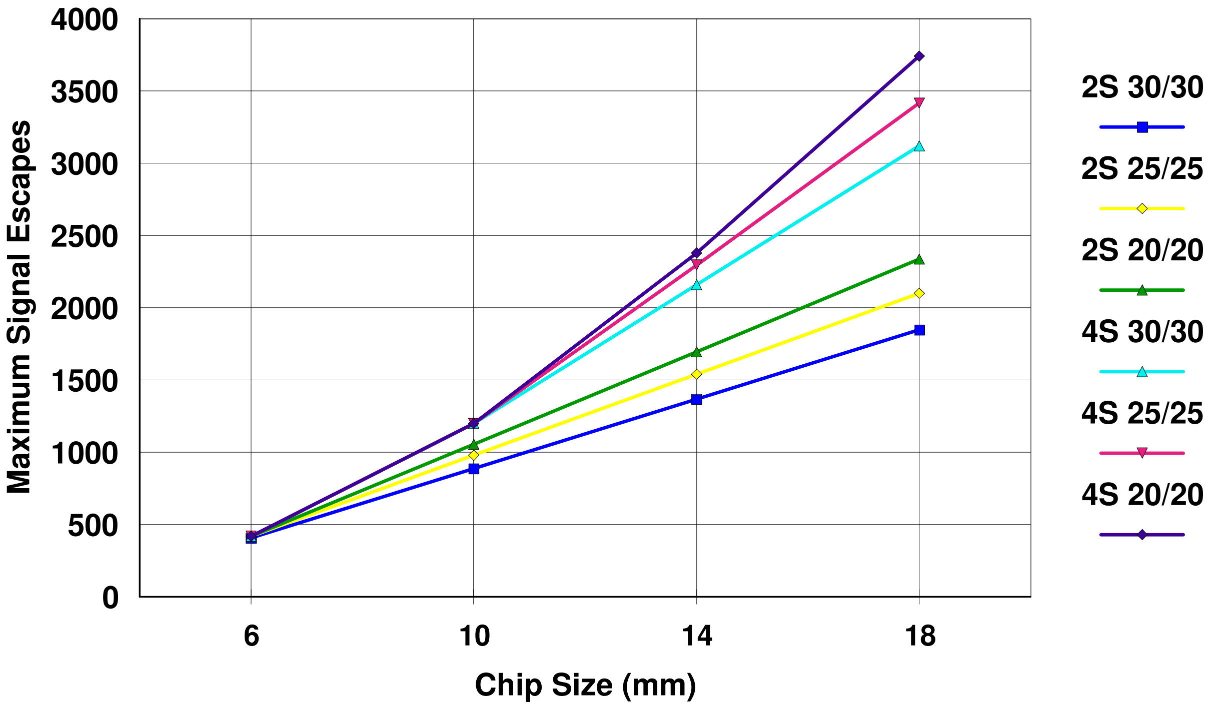

Figure 14 - Signal Escapes vs. Chip Size and Substrate Capability - 200 um C4 Pitch

Application Examples

With figure 14 established, it is useful to apply it to several examples and show how this information can be used to select substrates in support of chip properties. Assume that the chip functions demand 1000 signals and require a chip area of 12 mm by 12 mm. Looking at figure 14, two signals with 30 um lines and spaces can meet the requirement. This can become a target for substrate costing with six layer "Dense Core" substrates or ten layer standard core substrates as good alternatives. Next, assume that this same function can be processed with a finer chip technology and the total function can now fit on a 9 mm by 9 mm chip. This is a classical case of chip shrink. The two signal layer substrates are no longer capable of achieving escape without increasing chip size above 9 mm. Any of the four layer substrates will work and there is no reason to demand better density than 30 um lines and spaces because the corners contained most of the signal escapes. Another alternative is to stay with a two signal layer substrate (25 um lines and spaces) and increase the chip size from 9 mm to 10 mm. Total cost can be estimated to compare a 9 mm chip with a four signal layer substrate vs. a 10 mm chip with a two signal layer substrate. This result also allows a review of the actual chip footprint which is almost always different than the reference footprints shown here. If the actual chip footprint cannot achieve 1000 signals with a 9 mm x 9mm chip, perhaps the chip footprint needs to be revised so that maximum chip productivity can be achieved. The tables and curves above represent an existence theorem that can be a goal in actual designs.

Summary and Conclusions

The information shown in the above allows a chip designer to select the substrate that will be needed as soon as some fundamental chip parameters are defined. The process used in the analysis is to define a fundamental memo chip footprint that has no fundamental limitation to depth of signal wiring except for chip size and substrate capability. The next step is to define chip size vs. depth of signal wiring. Substrate design elements are defined next with two signal layer substrates and four signal layer substrates at variable line width and space.

The concept of "Dense Core" is introduced because it enables signal wiring on both the top and bottom halves of the substrate. The required core density to be a true "Dense Core" is defined and for the C4 pitches explored is below a 270 um pitch between holes. Although it is beyond the scope of this paper, "Dense Core" has demonstrated an improvement in power distribution performance [3] as well as more efficient use of layers for signal wiring.

Integration of all of this information produces a series of figures that can be used by the designer to determine the trade off between chip demands and substrate density requirements. Cost estimates and business cases can be made well in advance of actual designs to speed up the design cycle by targeting the chip and substrate designs to be consistent with these fundamental plots. Case studies of chips with multiple shrink cycles can be evaluated in advance and substrate technology selections can be made to enable chip shrink.

A key output of these plots is that smaller chips do not require very high substrate wiring capability because most of the signals are in the corner of the substrate. As chip size grows, the demand for higher signal complexity increases if signal wiring scales upward with chip size. Similarly, requirements for improvements in substrate feature sizes have their greatest impact as chip size grows and signal levels increase. In the best case, this fundamental information can be used to create a chip roadmap with a parallel substrate roadmap and permit qualification against this roadmap well in advance of actual designs.

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References

[1] T. Tsukada, S. Tsuchida, and Y. Mashimoto, "Surface Laminar Circuit and Flip Chip Attach Packaging", Proceedings of 7th International Microelectronics Conference, Yokohama, Japan, pp. 252-258, May 1992.

[2] T. Nishio, K. Kazushige, Y. Yamaji, N. Takahashi, K. Masanori, R. Malfatt, "An Approach to Reduce Build Up Layers for Flip Chip – Ball Grid Array (FC-BGA) Substrates", 2003 IEEE/CPMT/SEMI International Electronics Manufacturing Technology Symposium. Session 204, Paper 3, July 2003.

[3] J. Audet, D. O'Connor, M. Grinberg, and J. Libous, "Effect of Organic Package Core Via Pitch Reduction on Power Distribution Performance", Proceedings of 2004 Electronic Components and Technology Conference, pp. 1449-1453, June 2004.