Nano- and micro-filled conducting adhesives for *z*-axis interconnections: new direction for high-speed, high-density, organic microelectronics packaging

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Abstract

Purpose – The purpose of this paper is to discuss the use of epoxy-based conducting adhesives in *z*-axis interconnections.

Design/methodology/approach – A variety of conductive adhesives with particle sizes ranging from 80 nm to 15 μm were laminated into printed wiring board substrates. SEM and optical microscopy were used to investigate the micro-structures, conducting mechanism and path. The mechanical strength of the various adhesives was characterized by 90° peel test and measurement of tensile strength. Reliability of the adhesives was ascertained by IR-reflow, thermal cycling, pressure cooker test (PCT), and solder shock. Change in tensile strength of adhesives was within 10 percent after 1,000 cycles of deep thermal cycling (DTC) between -55 and 125°C.

Findings – The volume resistivity of copper, silver and low-melting point (LMP) alloy based paste were 5×10^{-4}, 5×10^{-5} and $2 \times 10^{-5}\,\Omega$ cm, respectively. Volume resistivity decreased with increasing curing temperature. Adhesives exhibited peel strength with Gould's JTC-treated Cu as high as 2.75 lbs/in. for silver, and as low as 1.00 lb/in. for LMP alloy. Similarly, tensile strength for silver, copper and LMP alloy were 3,370, 2,056 and 600 ψ, respectively. There was no delamination for silver, copper and LMP alloy samples after 3X IR-reflow, PCT, and solder shock. Among all, silver-based adhesives showed the lowest volume resistivity and highest mechanical strength. It was found that with increasing curing temperature, the volume resistivity of the silver-filled paste decreased due to sintering of metal particles.

Research limitations/applications – As a case study, an example of silver-filled conductive adhesives as a *z*-axis interconnect construction for a flip-chip plastic ball grid array package with a 150 μm die pad pitch is given.

Originality/value – A high-performance *Z*-interconnect package can be provided which meets or exceeds JEDEC level requirements if specific materials, design, and manufacturing process requirements are met, resulting in an excellent package that can be used in single and multi-chip applications. The processes and materials used to achieve smaller feature dimensions, satisfy stringent registration requirements, and achieve robust electrical interconnections are discussed.

Keywords Adhesives, Electronic engineering, Printed circuits, Semiconductor devices

Paper type Research paper

1. Introduction

The needs of the semiconductor marketplace continue to drive density into semiconductor packages. The high end of this market appears to be standard application-specific integrated circuits (ASICs), structured ASICs, and field-programmable gate arrays. These devices continue to need increasing signal, power, and ground die pads, and a corresponding decrease in pad pitch is required to maintain reasonable die sizes. The combination of these two needs is pushing complex semiconductor packaging designs. Traditionally, greater wiring densities were achieved by reducing the dimensions of vias, lines, and spaces, increasing the number of wiring layers and utilizing blind and buried vias. However, each of these approaches possess inherent limitations, for example, those related to drilling and plating of high-aspect ratio vias, reduced conductance of narrow circuit lines, and increased cost of fabrication related to additional wiring layers. Adding wiring layers offers a straightforward means of providing greater density of function in the package. However, added layers invariably translate to added cost. It is therefore imperative to make the most efficient use of real estate used for wiring in order to keep the number of wiring layers to a minimum. Packaging designs that are most effective in optimizing the use of available wiring space incorporate blind and buried vias. For interconnection with traditional plated through hole (PTH) technology, two PTHs are required to complete a circuit trace. PTHs consume real estate by blocking channels that could be used for wiring (Figure 1(a)). As via diameters decrease to accommodate more dense designs, plating of the vias becomes more of a challenge. This problem is alleviated to a degree by use of thinner, laser-friendly dielectric materials.

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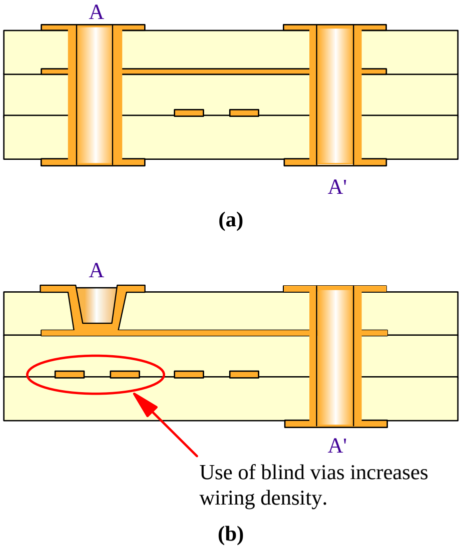
Figure 1 The use of blind vias increases wiring density in circuit layers below the via



Although the use of blind vias frees up wiring space, its utility is limited by the challenge of plating blind vias with aspect ratios (depth to diameter) greater than 1:1. Therefore, a means of fabricating a vertical interconnection that can be terminated at any wiring plane, at any depth, within the package is highly desirable. One method of extending wiring density beyond the limits imposed by these approaches is a strategy that allows for metal-to-metal *z*-axis interconnection of subcomposites during lamination to form a composite structure. Conductive joints can be formed during lamination using an electrically conductive adhesive. As a result, one is able to fabricate structures with vertically terminated vias of arbitrary depth. Replacement of conventional PTHs with vertically terminated vias opens up additional wiring channels on layers above and below the terminated vias and eliminates via stubs which cause reflective signal loss. Vertically terminated vias facilitate a more space-efficient package redesign for chips having a tighter pad pitch. In addition, parallel lamination of testable subcomposites offers yield improvement, shorter cycle times and ease of incorporating features conducive to high-speed data rates.

During the past few years, there has been increasing interest in using electrically conductive adhesives as interconnecting materials in the electronics industry (Liu, 1999; Liu *et al.*, 1995). Conductive adhesives are composites of a polymer and conductive fillers. Metal-to-metal bonding between conductive fillers provides electrical conductivity (Ye *et al.*, 1999; Yasuda *et al.*, 2003a, b, c), whereas a polymer resin provides better processability and mechanical robustness (Yao and Qu, 2002). Conductive adhesives usually have excess filler loadings that weaken the overall mechanical strength. Therefore, the reliability of the conductive joint formed between the conductive adhesive and the metal surface to which it is mated is of prime importance. Conductive adhesives can have broad particle size distributions and larger particles can be a problem when filling smaller holes (e.g. diameter of 60 μm or less), resulting in voids. Several nano- and micro-filled adhesives have been reported for advanced packaging applications. For example, Xiao and Chung (2005) describes epoxy or silicone based conductive adhesive joints and their thermal and mechanical stabilities. Jeong *et al.* (2005a) reported the effect of curing behaviours, solvent evaporation and shrinkage on the conductivity of adhesives. They (Jeong *et al.*, 2005b) also described the conductivity of micro-filled adhesives upon addition of nanoparticles. Lee *et al.* (2005) reported on the addition of nano-sized silver particles to micro-sized flakes and the effect on resistivity for these mixed-sized silver particle-filled conductive adhesives. Goh *et al.* (2006) mentioned the effect of annealing on the morphologies and conductivities of sub-micrometer sized nickel particles used for electrically conductive adhesive. Inoue and Suganuma (2006) investigated the variations in electrical properties of a typical isotropic conductive adhesive made with an epoxy-based binder that are caused by differences in the curing conditions. Coughlan and Lewis (2006) described electrical and mechanical analysis of conductive adhesives where the main properties of joint resistance and adhesive strength were examined before and after different environmental treatments. Fu *et al.* (2001) described cluster effects of nano fillers in conductive adhesives. Sancaktar and Dilsiz (1999) reported pressure-dependent conduction behaviour with particles of different sizes, shapes, and types. The effects of external pressure on the filler resistance were measured. Jiang *et al.* (2005) reported on surface functionalized nano-silver-filled conductive adhesives. Li *et al.* (2005) reported that self-assembled monolayers protected silver nano-particle-based conductive adhesives. These studies have described material properties and reliability assessment at a macroscopic level, but have not described device level fabrication, integration, and reliability issues. Although several composites are available for the advance of semiconductor technology, the authors believe that there is potential for improvement of the existing materials, so that flexible and reliable processes and material that can be processed at low temperatures can be developed for *z*-axis interconnections.

In the present study, adhesives formulated using controlled-sized particles, ranging from nanometer scale to micrometer scale, were used to fill small diameter holes to fabricate conductive joints for *Z*-interconnects. A variety of metals including Cu, Ag, and low-melting point (LMP) alloys have been used to make the conductive adhesives. The adhesive was applied onto copper substrates by printing or coating. This work also deals with adhesion issues between the adhesives and the substrates to which they are mated. The paper presents a reliability assessment of adhesive joints conducted by testing samples exposed to aging, pressure cooker tests (PCTs), IR-reflow, and solder shock. The work was extended to the development of a silver conductive adhesive filled *z*-axis interconnect construction for a flip-chip plastic ball grid array package (device) with a 150 μm die pad pitch. The structure employs an electrically conductive paste to interconnect thin cores (subcomposites). The cores were processed in parallel, aligned, and laminated to form a composite. The net effect is a composite laminate having vertical interconnections with small diameter holes that can terminate arbitrarily at any layer within the cross section of the package. There is no requirement for PTHs to be formed at the composite level. This effort is an integrated approach centering on three interrelated fronts:

1 materials development and characterization;
2 fabrication of packages; and

3 electrical performance and reliability at the component level.

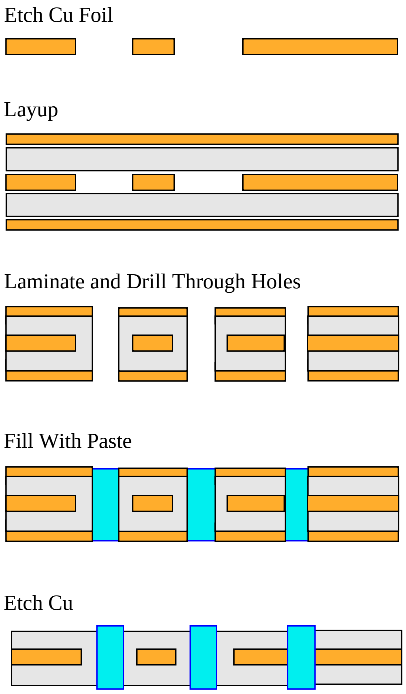
Reports of such an integrated approach to fabricate *Z*-interconnects for high-density, high-speed applications are not available in the literature.

2. Experimental procedure

A variety of silver, copper, and LMP-based nano and micro particles and their dispersion into epoxy resin were investigated in order to achieve uniform mixing in the adhesive. In a typical procedure, 88 g silver flakes, with an average particle size of 5 μm was mixed thoroughly with 12 g epoxy and made into a conducting paste. About 88 g silver nanoparticles, with average particle size 80 nm, required an additional 15 g propylene glycol methyl ether acetate solvent in order to make a conducting paste. The paste was deposited on a PWB substrate and cured at 190°C for 120 min using a heating rate 10°C/min. The process was extended for copper and LMP based systems where 88 g silver replaced by 88 g of 4 μm Copperand around 5 μm LMP – copper-mixed particles. For conductivity measurements, a thin film of this paste was deposited on a PWB substrate and cured at different temperatures ranging from 150 to 275°C. For reliability assessments, two paste films were laminated together at 190°C for 120 min at a heating rate 10°C/min.

For fabrication of a high-density laminate chip carrier, a 0S/1P joining core was constructed using a copper power plane, 35 μm thick, sandwiched between layers of a dielectric material composed of silica-filled allylated polyphenylene ether (APPE) polymer. Through holes in the joining cores, formed by laser drilling, and having diameters ranging from 50 to 75 μm, were filled with an optimized electrically conductive adhesive. Figure 2 shows flow chart of joining core processing.

Figure 2 Process flow chart to fabricate 0S/1P joining core



The adhesives were characterized by SEM and optical microscopy to ascertain the particle dispersion and interconnection mechanisms. A Keithley micro-Ωm was used for electrical characterization. Room temperature (25°C) viscosity was measured using a MALVERN C-VOR Rheometer in oscillation mode using 50 Pa stress at 1 Hz. The heat of reaction of the adhesives was studied using a differential scanning calorimeter (DSC). Practical adhesion (90° peel test) and tensile strength were measured using Instron (Model 1122) and MTS tensile testers, respectively.

3. Results and discussion

A conductive adhesive is a composite material consisting of a nonconductive polymer binder and conductive filler particles. When the filler content is high enough, the system is transformed into a good electrical conductor. Electrical conductivity of adhesives can be explained by two different theories:

1 percolation theory; and
2 tunneling effect or filled emission.

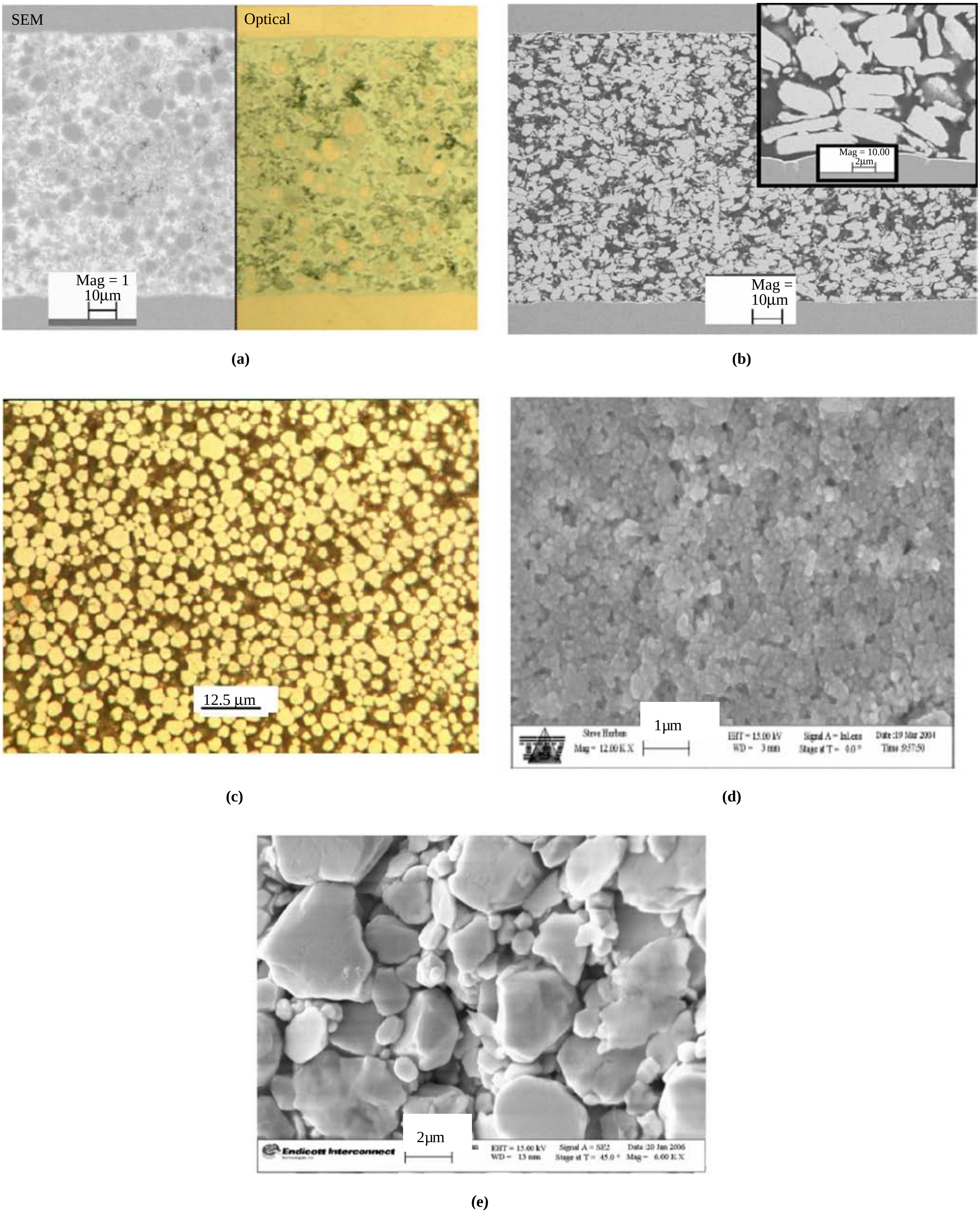
According to percolation theory, electrical connection is achieved primarily by inter-particle conduction. For electrical conduction, particles should make intimate physical contact and form a network (conductive chain), which helps in transfer of electrons. This conductive path is formed at a threshold volume fraction of conductive filler, which is a critical value at which all particles contact each other and form a conductive network in the resin (Wu *et al.*, 2006). This theory is related to the geometry of fillers, and neglects the influence of polymer matrix and type of fillers. For tunneling, electrons in one filler particle can hop/tunnel to the next particle through a potential barrier. Hopping is based on the distance between the particles and the size of the particles. According to the tunneling effect, total resistance of the conductive adhesive $R = R_c + R_b + R_t$, where R_c = contact resistance, R_b = intrinsic resistance of conductive particles, and R_t = tunneling resistance between particles. For micro particles, R_b is very small and its contribution to the total resistance is negligible. R_c is dependent on the diameter, *d*, of the contact spots. R_t is dependent on the distance, *a*, between the particles:

$$R_c = \frac{\sigma_c}{d} \quad [\sigma_c = \text{intrinsic filler resistivity}]$$

$$R_t = \frac{\sigma_t}{a} \quad [\sigma_t = \text{tunneling resistivity}]$$

The formation of a conduction path was observed by optical and SEM images of sample cross sections. Figure 3(A) shows a microstructure of a LMP-based adhesive. LMP melts and produces a continuous metallic network. In the silver adhesive, the average filler diameter is in the range of 5 μm. The filler loading was high and adjacent particles united mutually; necking phenomena between fillers occurred; namely, a conduction path was achieved (Ye *et al.*, 1999), as shown in Figure 3(B). A similar result was observed when silver particles were replaced by 4 μm Copperparticles (Figure 3(C)). A variety of silver filled adhesives with a mixture of nano- and micro-particles were studied. In nano-micro mixtures, nano-particles occupy interstitial positions to improve particle-particle contact for conductivity. For the silver-nano particles (~80 nm size), the fillers can self-sinter

Figure 3 SEM and optical micrographs of adhesives: (A) low melting point (LMP) alloys; (B) silver micro particles; (C) Coppermicro particles; (D) silver-nano particles; and (E) mixture of silver-nano and micro particles



and make a continuous conduction path. Because of the high-surface area of silver nano-particles, an excess amount of solvent is required to make a high-loading silver paste. Figures 3(D) and 3(E) show microstructures of nano-silver filled and nano-micro silver filled adhesives.

Conducting adhesives cured at ~190°C for 2 h showed low-volume resistivity. The volume resistivity of copper, LMP and silver paste are 5×10^{-4}, 5×10^{-5} and $2 \times 10^{-5}\,\Omega$ cm, respectively. All adhesives fabricated from LMP and copper epoxy nano-composites showed a resistivity of about 10^{-4} to $10^{-5}\,\Omega$ cm, whereas silver adhesives showed resistivity of about 10^{-4} to $10^{-6}\,\Omega$ cm. Silver nano-particles showed volume resistivity in the range of $10^{-4}\,\Omega$ cm and the resistivity decreased to $10^{-5}\,\Omega$ cm when nano-micro mixtures were used. Figure 3 and resitivity data support the tunneling theory more than the percolation theory. According to percolation theory, silver, copper and LMP should have similar resistivities at the same loading. But tunneling theory with different R_c, R_b, R_t could be more appropriate to describe different resistivity of different paste. For example, the resistivity of micro silver particle paste is lower than nano-particle paste. For micro-particle paste, resistivity depended upon R_c only but nano-silver paste counts all three resistances, i.e. R_c, R_b, R_t. The resistivity is minimum for the silver paste. Volume resistivity decreases with increasing curing temperature due to sintering of metal particles. Figure 4 shows the volume resistivity of silver paste as a function of curing temperature. There is a significant resistivity drop with increasing curing temperature from 150 to 175°C. Figure 5 shows the volume resistivity of silver adhesive with aging as a function of curing temperature. The resistivities of adhesives after 72 h aging and cured at 150, 190, 265°C were 50×10^{-5}, 32×10^{-5} and $2 \times 10^{-5}\,\Omega$ cm, respectively. The change in resistivity with aging was significant when cured below 200°C, but it was not significant when cured at or above 250°C. A sharp increase is observed up to 24 h, and thereafter it increases slowly. Adhesive viscosity increased with time at room temperature (25°C), around 10 and 30 percent viscosity increase from 0 to 20 h and 40 h, respectively. Viscosity is more than double after 70 h. Heat of reaction, calculated from DSC, was changed from 49 J/g after 1 hr to 31 J/g after 24 h. It reduces to 10 J/g after 90 h at room temperature (25°C). The changes in viscosity and corresponding heat of reaction indicate that the adhesive slowly cured at room temperature and the partially cured resin increased the overall resistivity when cured below 200°C. Above 250°C, particle sintering plays an important role in maintaining low-volume resistivity or high conductivity. The sinterability of the silver adhesive was further evaluated using high-temperature curing. Here, we have used a mixture of nano and micro silver particles. Figure 6 shows the microstructure of adhesive cured at 275°C. At 190°C, conductivity is achieved through particle-particle connection (Figure 3). A continuous metallic network results when the adhesive is cured at 275°C.

Figure 4 Volume resistivity of silver adhesive as a function of curing temperatures

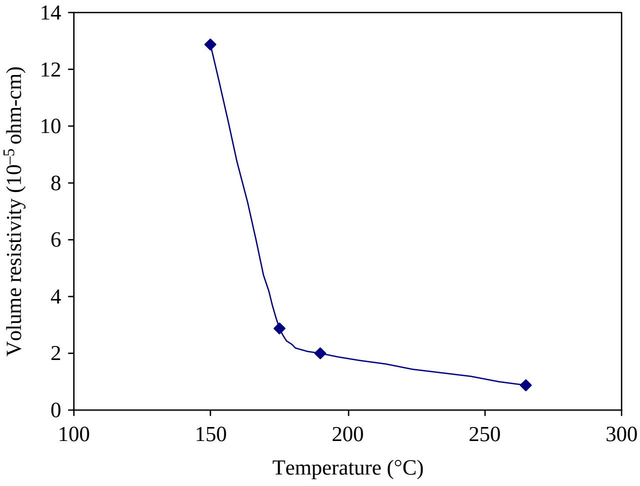
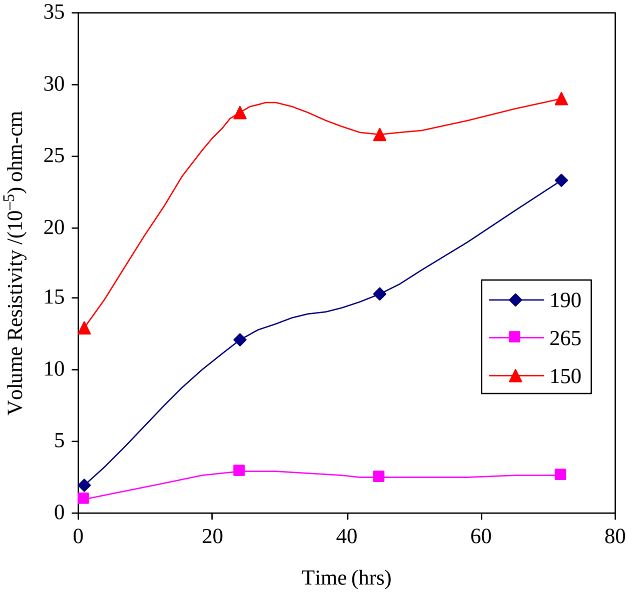
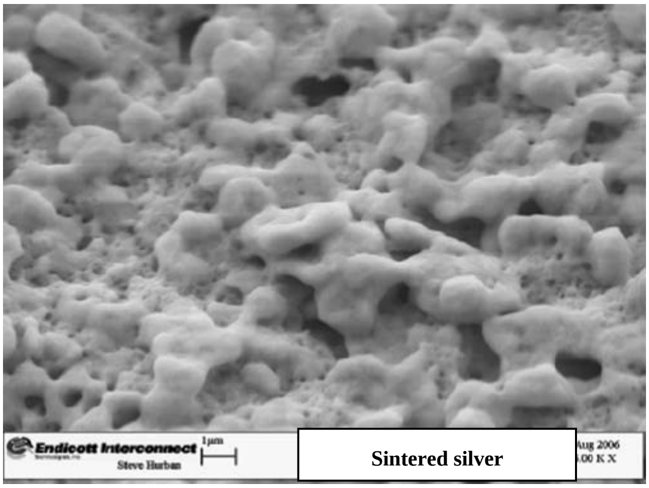


Figure 5 Volume resistivity of silver adhesive with aging as a function of curing temperature



Adhesion between the adhesive and the substrate to which it is mated is critical to the reliability of a semiconductor package. The bond strength of adhesive joints was evaluated

Figure 6 SEM images for the nano-micro adhesive cured at 275°C



using 90° peel test and tensile strength measurements. Adhesives exhibited peel strength as high as 2.75 lbs/in. for silver, and as low as 1.00 lb/in. for LMP alloy. Similarly, tensile strength for silver, copper and LMP alloy were 3,370, 2,056 and 600 ψ, respectively. All adhesives showed cohesive failure at the interface. Table I summarizes the 90° peel strength and tensile strength of conductive adhesives. Among all, silver-based adhesives showed the highest mechanical strength.

Conductive adhesives are of little value in electronic packaging unless they can survive the rigors of testing those modules or boards receive. To test the reliability of joints formed using conductive adhesives, a film of adhesive about 100 μm thick was laminated between two copper substrates. The adhesive film was surrounded by a 100 μm thick layer of glass cloth-reinforced dielectric (pre-preg). The surrounding 100 μm thick dielectric helped to maintain proper adhesive thickness during lamination. Reliability of the laminate was ascertained by PCT, solder shock, and IR-reflow. For PCT, samples were exposed to 100 percent humidity with a constant pressure of 19 ψ at 121°C. Table II summarizes test results. The changes in tensile strength of the adhesives was within 10 percent after 1,000 cycles of deep thermal cycling (DTC) between -55 and 125°C. Samples were stable after reliability testing and there was no delamination after PCT, solder shock and IR-reflow. Laminates were also exposed to PCT (4 h) followed by a 15 s of solder dip at 260°C.

Reliable metal-epoxy adhesives were used for hole fill applications to fabricate *z*-axis interconnections in laminates. Figure 7 shows LMP, copper and silver adhesive-filled joining cores as representative examples. Holes having a diameter of roughly 55 μm, with an aspect ratio of about 3 to 1, were filled with different pastes. All pastes had continuous connection from top to bottom. LMP melted and grew as a big grain and separate organics (black regions). Copper and silver both maintain their particle-particle connection mechanism and also maintain paste uniformity in the holes. Thus, it is possible to make a wide variety of conductive adhesives that can be used for *z*-axis interconnection by way of holes in the joining cores. The reliability of conductive joints in the test vehicle was further examined by testing via 1,000 cycles DTC, IR-reflow (3X, 225°C), PCT and solder shock. No intrinsic failure mechanisms were observed and there was no delamination. Conductive joints were stable even

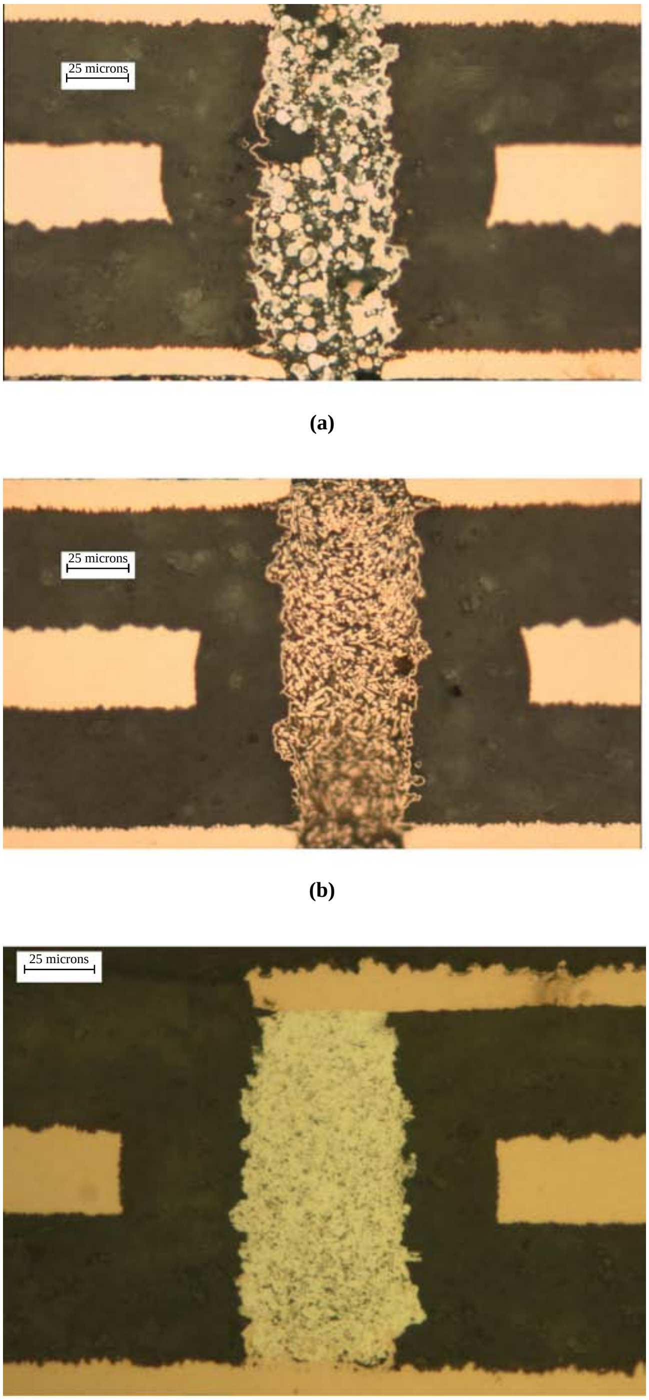
Table I 90° peel-strength and tensile strength of adhesives

Adhesive	90° peel strength (lbs/in.)	Tensile strength (ψ)	Failure mode
LMP alloy	1	600	Cohesive
Copper (Cu)	1.77	2,056	Cohesive
Silver (Ag)	2.75	3,370	Cohesive

Table II Reliability test results

Tests	Silver adhesive	Copper adhesive	LMP adhesive
IR-Reflow (3X reflows at 225°C)	Passed	Passed	Passed
PCT (4 h) (121°C/100 percent RH)	Passed	Passed	Passed
Solder Shock (15 s dip at 260°C)	Passed	Passed	Passed
IR-reflow + PCT + solder shock (3X reflows + 121°C/100 percent RH + 15 s solder dip at 260°C)	Passed	Passed	Passed
IR-reflow + solder (3X reflows + 15 s solder dip at 260°C)	Passed	Passed	Passed

Figure 7 Adhesive-filled joining cores: (A) LMP; (B) copper; and (C) silver



(a)

(b)

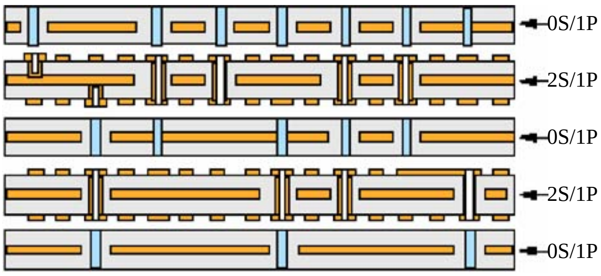
(c)

after multiple IR-reflow (3X) followed by multiple (3X) 15 s solder dips.

Integral to the methodology described in this paper is the use of core building blocks that can be laminated in a manner such that electrical interconnection between adjacent cores is achieved. The cores can be structured to contain a variety of arrangements of signal, voltage, and ground planes. In addition, signal, voltage, and ground features can reside on the same plane. As a case study, this *Z*-interconnection methodology was used to fabricate a package for a flip chip device having a pad pitch of 150 μm. Two basic building blocks were used for this case study (Figure 8). One was a 2S/1P core in which the internal power plane (P), a 35 μm thick copper foil, was sandwiched between two layers of a PTFE-based dielectric. The internal signal (S) layers comprised copper features generated using a semi-additive (pattern plating) process. A line thickness of 12 μm was achieved with minimum dimensions for line width and space of 25 μm each. The second building block in this case study was a 0S/1P core. This core is constructed using a copper power plane, 35 μm thick, sandwiched between layers of a dielectric material composed of a silica-filled APPE polymer. Through holes in the core were filled with an electrically conductive adhesive. By alternating 2S/1P and 0S/1P cores in the lay-up prior to lamination, the conductive paste electrically connects the copper pads on the 2S/1P cores that reside on either side of the 0S/1P core. Two signal layers are added to the composite structure each time one adds an additional 2S/1P core and an additional 0S/1P core. A structure with four signal layers composed of five subcomposites (two 2S/1P cores and three 0S/1P cores) is shown schematically in Figure 8. Although this particular construction comprises alternating 2S/1P and 0S/1P cores, it is possible to place multiple 0S/1P cores adjacent to each other in the stack.

Figure 8 Parallel lamination of subcomposites (cores) to form laminate chip carrier having four signal wiring planes with a stripline transmission line structure

Fabrication of core building blocks.....



with parallel lamination to produce a
4S laminate chip carrier.....

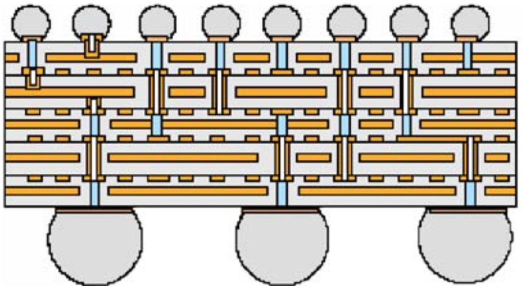


Figure 9 shows optical photographs and SEM micrographs of a joining core having paste-filled holes with a diameter of 55 μm. It can be seen that the conductive adhesive in the filled hole protrudes above the surface of the surroundings dielectric (see especially Figure 9 (D)). The protruding paste helps to produce robust conductive joint between two 2S/1P cores during the composite lamination process. The adhesive-filled joining cores were laminated with circuitised subcomposites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide *Z*-interconnection among the circuitised subcomposites. A photograph of a composite laminate structure is shown in cross section in Figure 10.

The *Z*-interconnect package technology in this study uses the same high-performance material set previously established in another chip package technology to yield excellent reliability and electrical performance (McBride *et al.*, 2003; Budell *et al.*, 2001; Alcoe *et al.*, 2000). In addition to making wiring channels available, this *Z*-interconnection technology reduces losses for high-speed signals. PTHs have been replaced with blind and buried vias, reducing or eliminating via stubs (Figure 11).

For the laminate of the present investigation, the average CTE of the composite was 18.3 ppm/°C. This is comparable to that of copper and adhesives, 17 ppm/°C, whereas the CTE of the silica-filled PTFE is 25 ppm/°C, and that of silica-filled APPE is 41 ppm/°C. It is apparent that the CTE of the laminate structure is dominated by that of the copper planes and adhesive joints in the composite cross section.

The test vehicle for component level stress testing was a chip carrier having a flip chip die pad pitch of 150 μm. The die size was 9.3 mm^2 owing to the limitation of the BGA I/O (pitch and substrate body size) and the die pad pitch. The body size (package outer dimensions) was 52.5 mm^2 with a 1 mm BGA pad pitch.

Assembled components (chip on composite) were subjected to JEDEC Level four preconditioning per the following conditions:

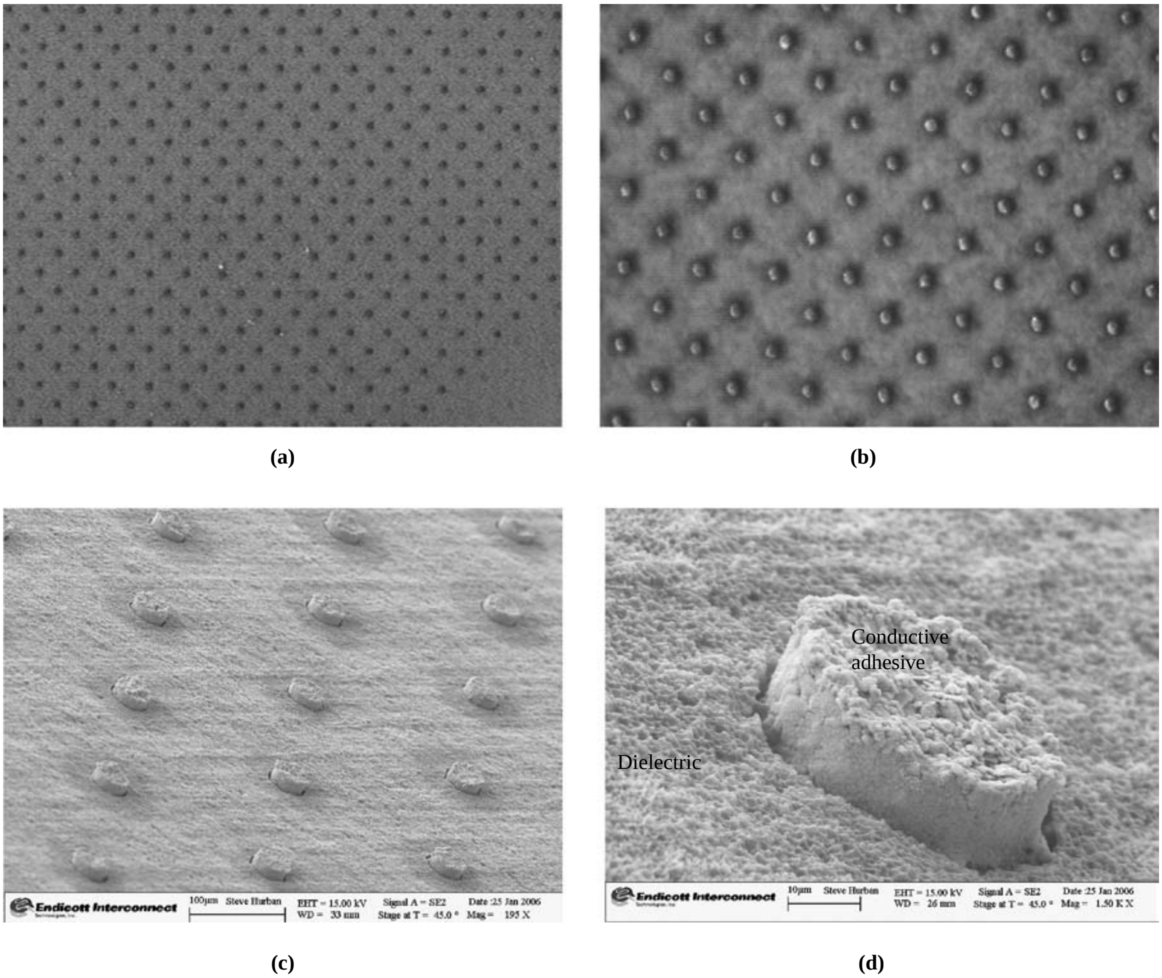
1. 5 cycles from -40 to $+60$°C;
2. 24 h at 125°C;
3. 96 h at 30° and 60 percent RH; and
4. 3X reflows, 225°C peak.

Components were then subjected to environmental stress testing using the tests and conditions outlined in Table III. No intrinsic failure mechanisms were observed. There was no die cracking, underfill delamination, BGA ball fatigue, dielectric cracking, or delamination.

4. Conclusions

In conclusion, a variety of nano-and micro-filled copper, silver and LMP-based conducting adhesives were used for a *z*-axis interconnection application. High-aspect ratio, small diameter (~55 μm) holes were successfully filled. Silver-filled adhesives were electrically and mechanically better than copper- and

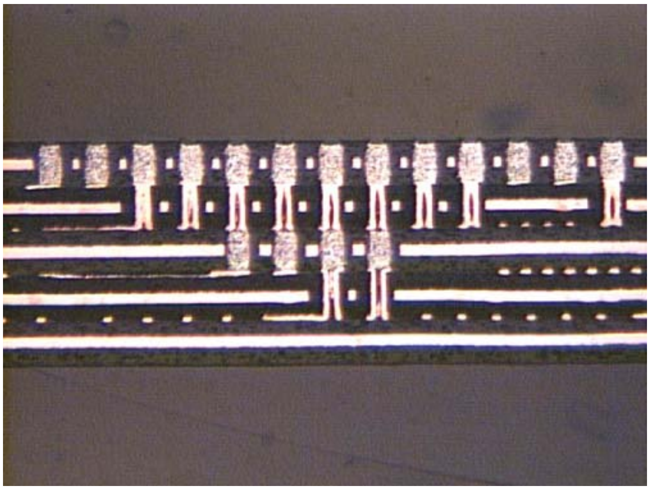
Figure 9 Photographs of adhesive filled joining core: (A) Large area optical photograph; (B) higher magnification optical photograph; (C) corresponding low magnification SEM micrograph; and (D) higher magnification SEM micrograph



(a) (b)

(c) (d)

Figure 10 Photograph of *Z*-interconnect laminates shown in cross section



LMP-filled adhesives. All adhesives maintained high-tensile strength even after 1,000 cycles DTC. Conductive joints were stable after 3X IR-reflow, 1,000 cycles DTC, PCT, and solder shock. The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide stable, reliable *Z*-interconnections among the circuitized subcomposites.

A high-performance *Z*-interconnect package can be provided which meets or exceeds JEDEC level requirements if specific materials, design, and manufacturing process requirements are met, resulting in an excellent package that can be used in single and multi-chip applications. By designing an organic package without electrical stubs and without through holes, high-wiring density and excellent electrical performance can be achieved. Novel means of providing vertical electrical interconnection in organic substrates can help semiconductor packaging keep pace with the needs of the semiconductor marketplace.

Figure 11 Ability to terminate vias at any internal layer (bottom) provides additional channels for wiring and reduces or eliminates stubs associated with PTHs (top)

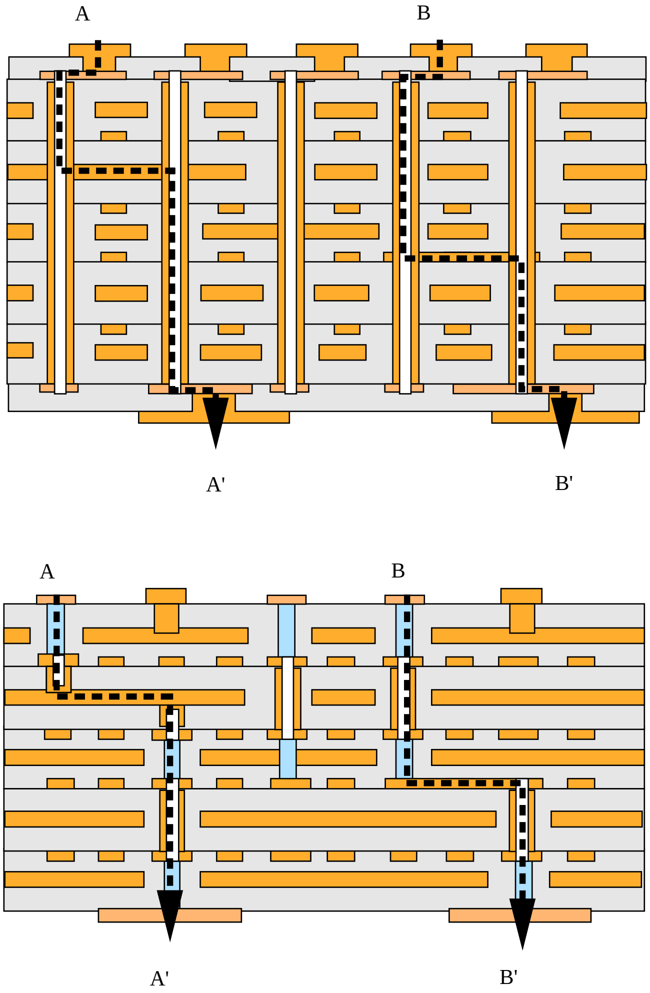


Table III Stress testing conditions

Test	Conditions	Duration
Accelerated thermal cycling (component on card with heat sink)	0 to 100°C BLR	3,600 cycles
DTC	− 40 to 125°C	1,000 cycles
High temperature storage	150°C	1,000 h
PCT	121C/100 percent RH/2 atm	96 h
Wet thermal shock	− 55 to 125°C	1,000 cycles

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